Ordering number : EN8590A

2SJ665

P-Channel Power MOSFET
−100V, −27A, 77mΩ, TO-263-2L

ON Semiconductor®
http://onsemi.com

Features

- ON-resistance $R_{DS}(on)1$=59mΩ(typ.)
- 4V drive
- Input capacitance Ciss=4200pF (typ.)

Specifications

Absolute Maximum Ratings at Ta=25°C

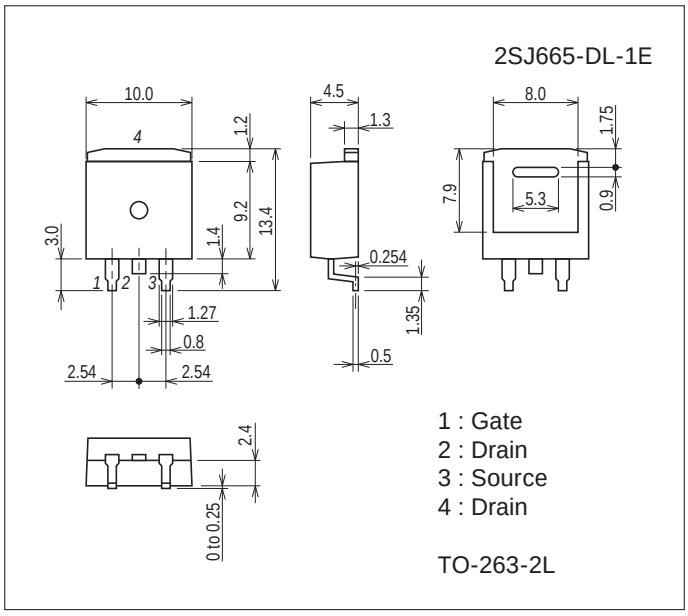
Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		−100	V
Gate-to-Source Voltage	V_{GSS}		±20	V
Drain Current (DC)	I_D		−27	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	−108	A
Allowable Power Dissipation	P_D	Tc=25°C	65	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C
Avalanche Energy (Single Pulse) *1	E_{AS}		48	mJ
Avalanche Current *2	I_{AV}		−27	A

Note :*1 V_{DD}=−30V, L=100μH, I_{AV}=−27A (Fig.1)
*2 L≤100μH, single pulse

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

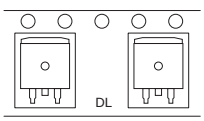
unit : mm (typ)
7535-001



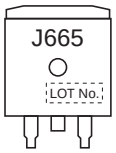
Product & Package Information

- Package : TO-263-2L
- JEITA, JEDEC : SC-83, TO-263
- Minimum Packing Quantity : 800 pcs./reel

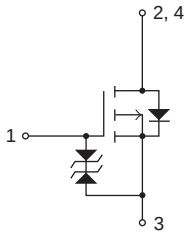
Packing Type: DL



Marking



Electrical Connection



Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−1mA, V_{GS}=0V	−100			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=−100V, V_{GS}=0V			−1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=−10V, I_D=−1mA	−1.2		−2.6	V
Forward Transfer Admittance	| yfs |	V_{DS}=−10V, I_D=−14A	15	25		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=−14A, V_{GS}=−10V		59	77	mΩ
	R_{DS}(on)2	I_D=−14A, V_{GS}=−4V		75	105	mΩ
Input Capacitance	Ciss	V_{DS}=−20V, f=1MHz		4200		pF
Output Capacitance	Coss			280		pF
Reverse Transfer Capacitance	Crss			220		pF
Turn-ON Delay Time	t_d(on)	See Fig.2		30		ns
Rise Time	t_r			150		ns
Turn-OFF Delay Time	t_d(off)			330		ns
Fall Time	t_f			135		ns
Total Gate Charge	Qg	V_{DS}=−50V, V_{GS}=−10V, I_D=−27A		74		nC
Gate-to-Source Charge	Qgs			12.8		nC
Gate-to-Drain “Miller” Charge	Qgd			14.7		nC
Diode Forward Voltage	V_{SD}	I_S=−27A, V_{GS}=0V		−0.98	−1.2	V

Fig.1 Avalanche Resistance Test Circuit

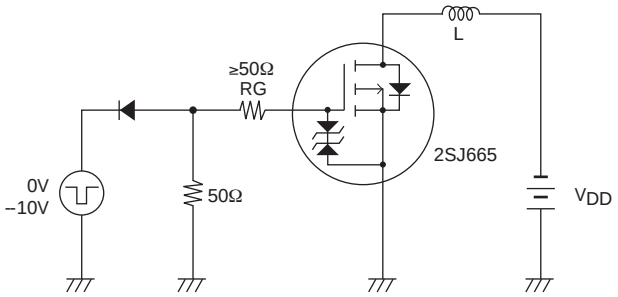
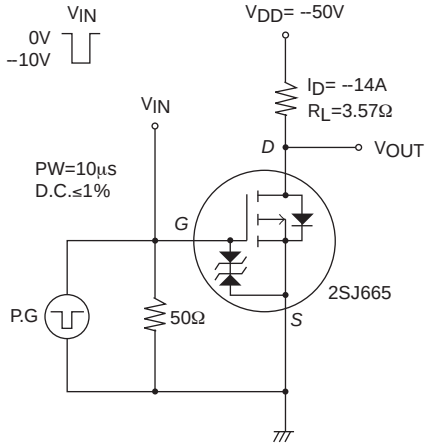
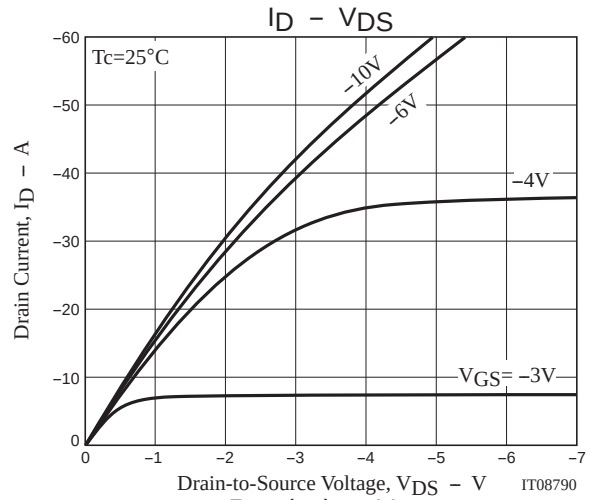


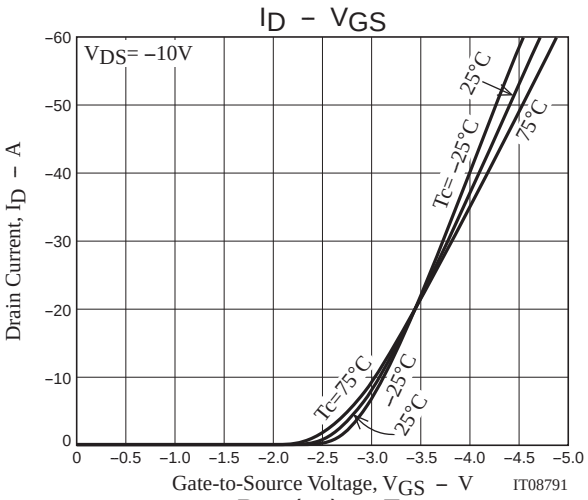
Fig.2 Switching Time Test Circuit

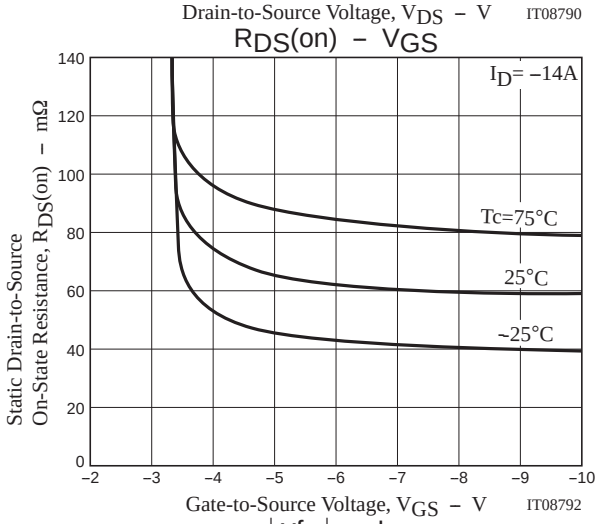


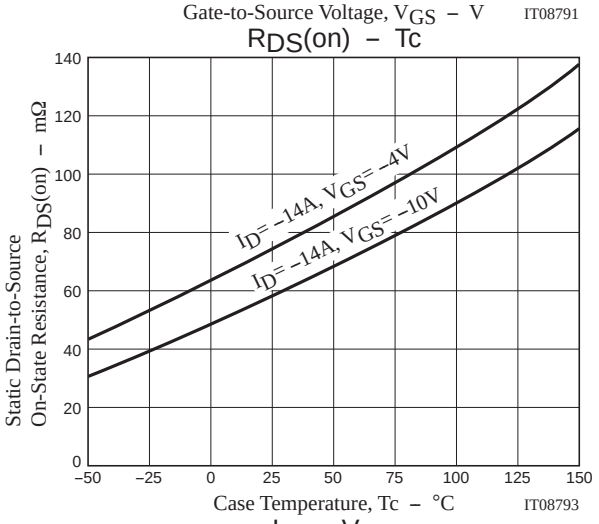
Ordering Information

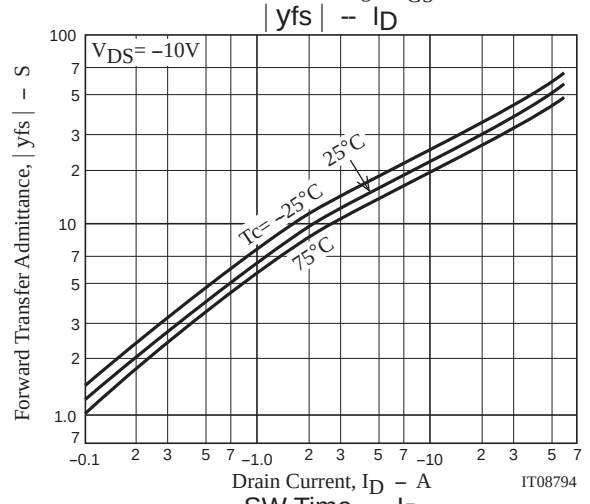
Device	Package	Shipping	memo
2SJ665-DL-1E	TO-263-2L	800pcs./reel	Pb Free

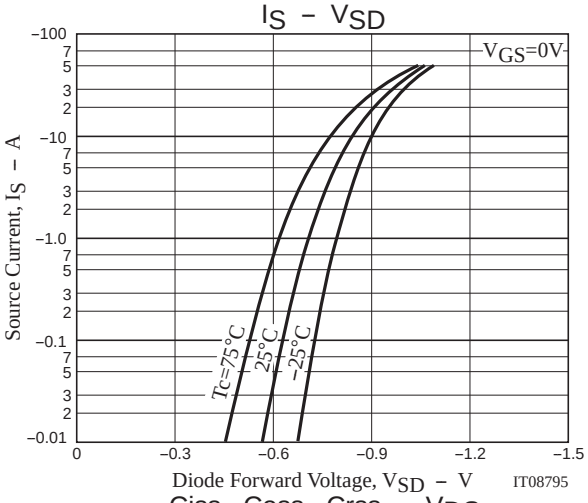

ID – VDS
Tc=25°C
–10V
–6V
–4V
VGS= –3V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT08790

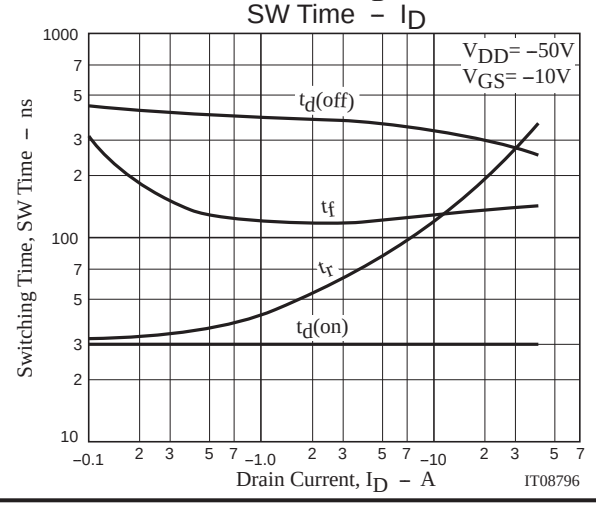

ID – VGS
VDS= –10V
Tc= –25°C
25°C
75°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT08791

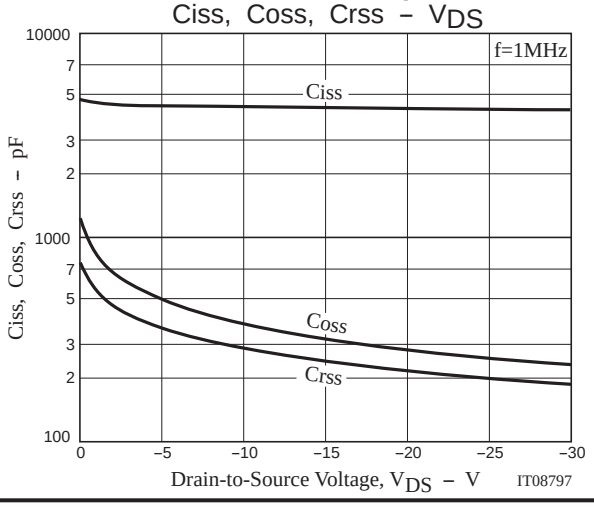

RDS(on) – VGS
ID= –14A
Tc=75°C
25°C
–25°C
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT08792

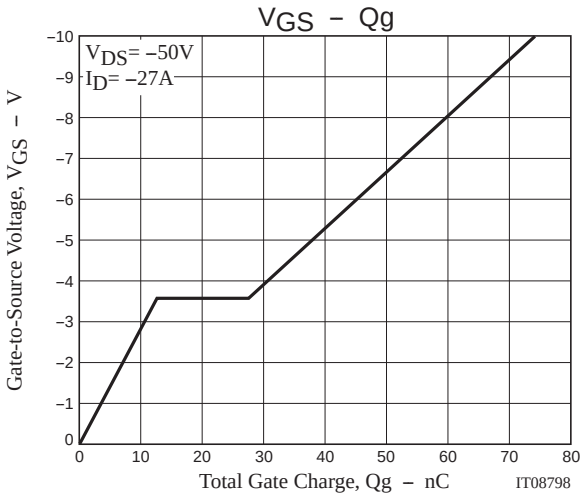

RDS(on) – Tc
ID= –14A, VGS= –4V
ID= –14A, VGS= –10V
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Case Temperature, Tc – °C
IT08793

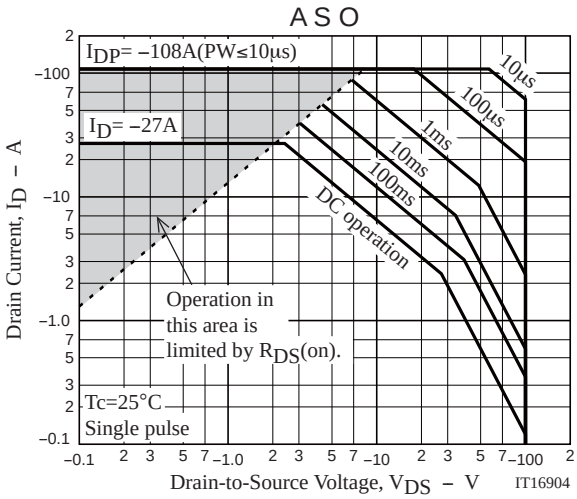

| yfs | – ID
VDS= –10V
Tc= –25°C
25°C
75°C
Forward Transfer Admittance, | yfs | – S
Drain Current, ID – A
IT08794

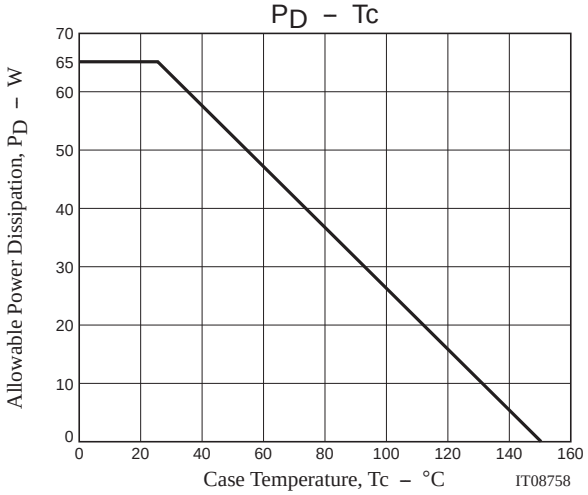

IS – VSD
VGS=0V
Tc=75°C
25°C
–25°C
Source Current, IS – A
Diode Forward Voltage, VSD – V
IT08795


SW Time – ID
VDD= –50V
VGS= –10V
td(off)
tf
tr
td(on)
Switching Time, SW Time – ns
Drain Current, ID – A
IT08796


Ciss, Coss, Crss – VDS
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT08797


VGS – Qg
VDS= –50V
ID= –27A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT08798


A S O
IDP= –108A(PW≤10μs)
ID= –27A
10μs
100μs
1ms
10ms
100ms
DC operation
Operation in this area is limited by RDS(on).
Tc=25°C
Single pulse
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT16904


PD – Tc
Allowable Power Dissipation, PD – W
Case Temperature, Tc – °C
IT08758

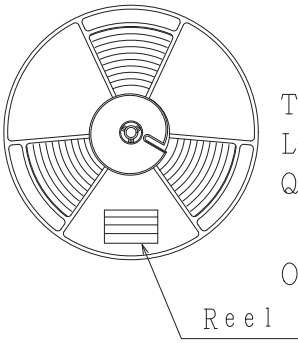
Taping Specification

2SJ665-DL-1E

1. Packing Format

Package Name	Maximum Number of devices contained (pcs)			Packing format	
	Reel	Inner box	Outer box	Inner BOX	Outer BOX
TO-263-2L	800	1600	6400	SPD-0V0011 2 reel contained Dimensions:mm(external) 351×340×68	SPD-0V0009 4 inner boxes contained Dimensions:mm(external) 390×370×318

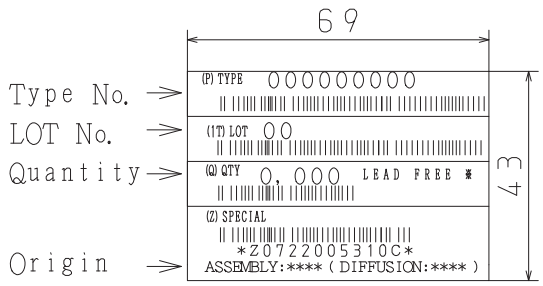
Packing method



Reel label

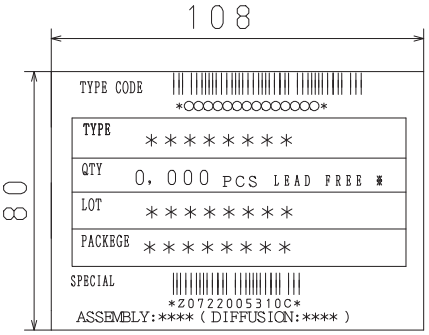
Reel label, Inner box label

(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.

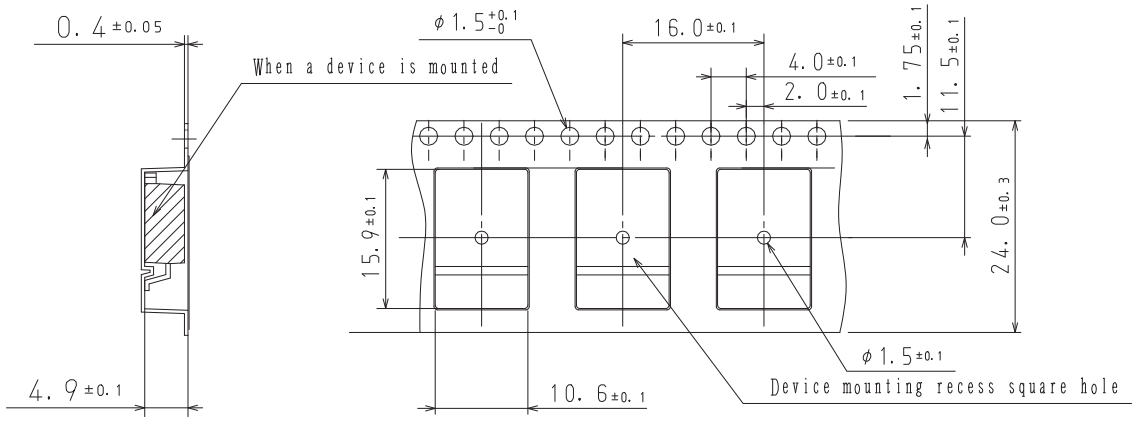


NOTE (1)
The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

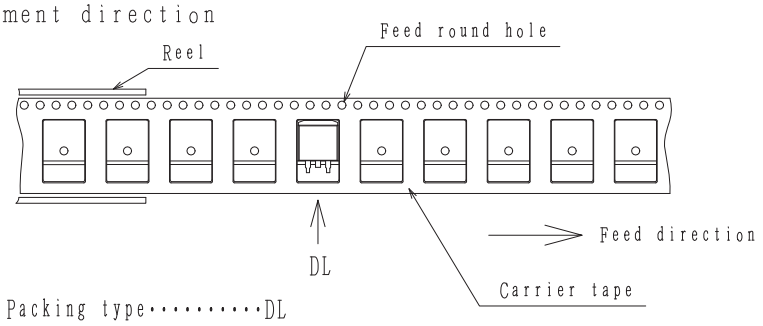
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A

2. Taping configuration

2-1. Carrier tape size (unit:mm)

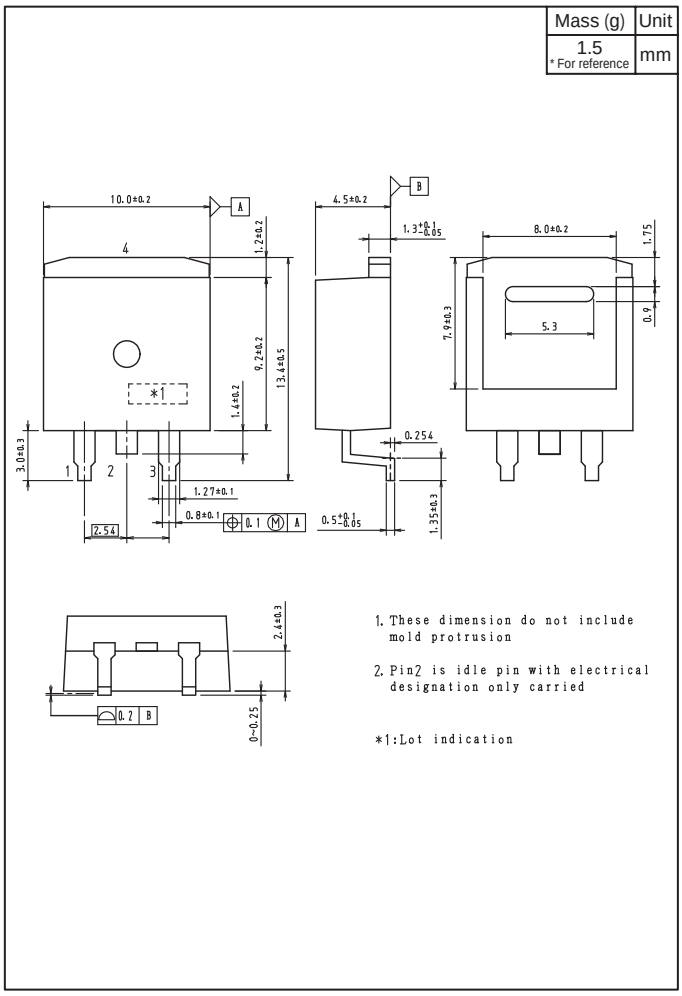


2-2. Device placement direction

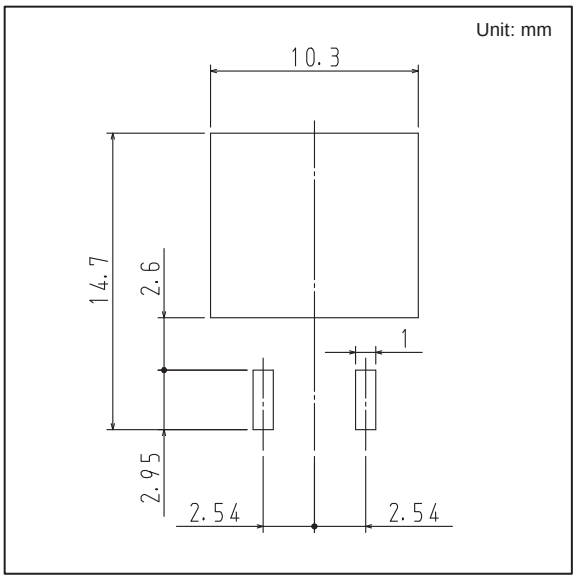


Outline Drawing

2SJ665-DL-1E



Land Pattern Example



Note on usage : Since the 2SJ665 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.