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2N5754-2N5757

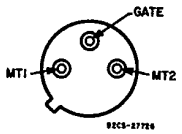
2.5-A Silicon Triacs

Features:

- *Gate sensitivity - 25 mA*
- *di/dt capability - 100 A/μs*
- *Low switching losses*
- *Low-on-state voltage at high current levels*

Package \ Voltage	100 V Types	200 V Types	400 V Types	600 V Types
Modified TO-205	2N5754	2N5755	2N5756	2N5757

TERMINAL DESIGNATIONS



MODIFIED TO-205

These RCA triacs are gate-controlled full-wave silicon ac switches that are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate triggering voltages.

The gate sensitivity of these triacs permits the use of economical transistorized control circuits and enhances their use in low-power phase control and load-switching applications.

MAXIMUM RATINGS, *Absolute-Maximum Values:*
For operation with sinusoidal supply voltage at frequencies up to 50/60 Hz and with resistive or inductive load

	2N5754	2N5755	2N5756	2N5757	
* V_{DROM} Δ					
Gate open, T_J = -65 to 100°C	100	200	400	600	V
$I_{T(RMS)}$ (θ = 360°C)					
T_C = 70°C	2.5				A
For other conditions	See Figs. 2, 3, 4				
I_{TSM}					
For one cycle of applied principal voltage, at current and temperature shown above for $I_{T(RMS)}$					
* 60 Hz (sinusoidal)	25				A
50 Hz (sinusoidal)	21				A
For more than one cycle of applied principal voltage	See Figs. 5, 6				
di/dt					
$V_D = V_{DROM}$, I_{GT} = 50 mA, t_r = 0.1 μs	100				A/μs
I^2t [At T_C shown for $I_{T(RMS)}$]					
t = 20 ms	4.3				A^2s
t = 2.5 ms	2				A^2s
t = 0.5 ms	1				A^2s
For other time values	See Fig. 6				
* I_{GTM} •					
For 1 μs max.	1				A
P_{GM}					
Peak (For 1 μs max., $I_{GT} \leq 1$ A (peak)	10				W
* $P_{G(AV)}$ - T_C = 70°C	0.15				W
T_A = 25°C	0.05				W
* T_{stg}	-65 to 150				°C
* T_C	-65 to 100				°C
T_T					
During soldering for 10 s maximum at distance ≥ 1/16 in. (1.58 mm) from seating plane	225				°C

For Notes See Electrical Characteristic Chart

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ELECTRICAL CHARACTERISTICS, At Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature (T_C)

	CHARACTERISTICS	LIMITS			UNITS
		ALL TYPES			
		MIN.	TYP.	MAX.	
•	I_{DROM} Δ Gate open, T_J = 100°C, V_{DROM} = Max. rated value	—	0.2	0.75	mA
•	V_{TM} Δ (See Fig. 7) I_T = 10 A (peak), T_C = 25°C I_T = 3.5 A (peak), T_C = 25°C	— —	2.2 —	2.6 1.8	V
	I_{HO} Δ (See Fig. 8) Gate open, Initial principal current = 150 mA (dc), V_D=12 V T_C = 25°C T_C = -65°C	 — —	 6 20	 35 82 *	mA
•	dv/dt (Commutating) Δ $V_D = V_{DROM}$, $I_{T(RMS)}$ = 2.5A commutating di/dt = 1.33 A/ms, gate unenergized, T_C = 70°C	0.5	—	—	V/μs
	dv/dt (Off-State) Δ $V_D = V_{DROM}$, exponential voltage rise, gate open, T_C = 100°C	10	100	—	V/μs
	I_{GT} Δ • V_D = 12 V dc, R_L = 30 Ω, T_C = 25°C Mode V_{MT2} V_G I+ positive positive III- negative negative I- positive negative III+ negative positive	 — — — —	 5 5 10 10	 25 25 40 40	mA
	V_D = 12 V dc, R_L = 30 Ω, T_C = -65°C Mode V_{MT2} V_G I+ positive positive III- negative negative I- positive negative III+ negative positive	 — — — —	 30 30 40 40	 60 * 60 * 100 * 100 *	
	V_{GT} Δ • (See Fig. 10) V_D = 12 V dc, R_L = 30 Ω, T_C = 25°C V_D = 12 V dc, R_L = 30 Ω, T_C = -65°C $V_D = V_{DROM}$, R_L = 125 Ω, T_C = 100°C	 — — 0.2	 0.9 1.5 —	 2.2 3 * —	V
	t_{gt} $V_D = V_{DROM}$, I_G = 60 mA, t_r = 0.1 μs, I_T = 10 A (peak) T_C = 25°C	—	1.8	2.5	μs
•	$R\theta_{JC}$ Steady-State	—	—	8.5	°C/W
	$R\theta_{JA}$ Steady-State	—	—	150	

* In accordance with JEDEC registration data format JS-14, RDF-2 - filed for the JEDEC (2N-Series) types.
Δ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
• For either polarity of gate voltage (V_G) with reference to main terminal 1.

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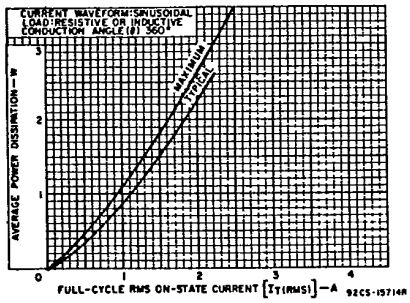


Fig. 1 - Power dissipation vs. on-state current.

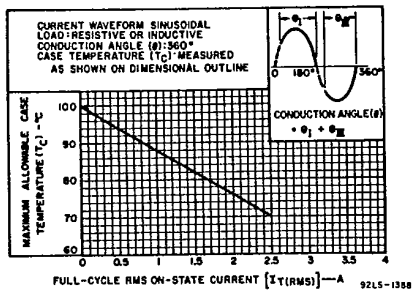


Fig. 2 - Maximum allowable case temperature vs. on-state current.

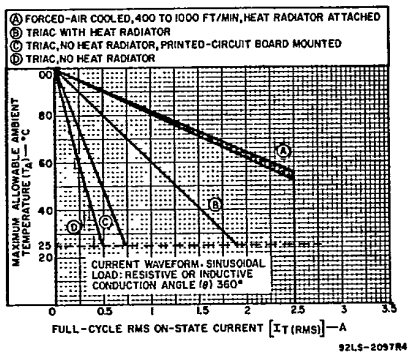


Fig. 3 - Maximum allowable ambient temperature vs. on-state current.

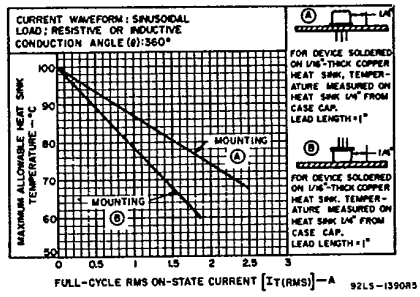


Fig. 4 - Maximum allowable heat-sink temperature vs. on-state current.

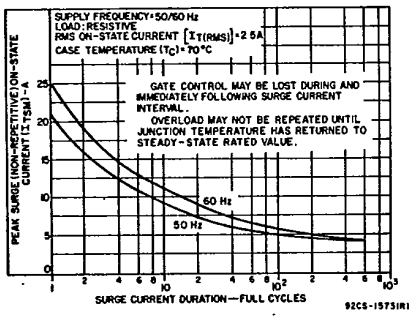


Fig. 5 - Peak surge on-state current vs. surge-current duration.

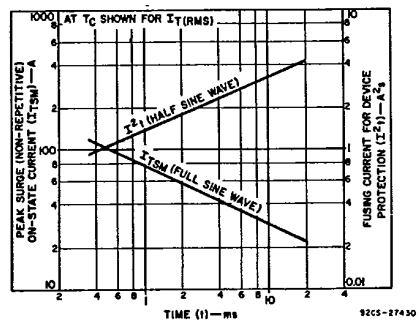


Fig. 6 - Peak surge on-state current and fusing current vs. time.

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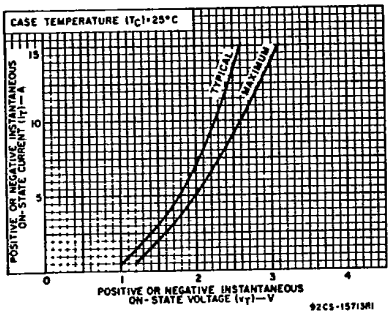


Fig. 7 - On-state current vs. on-state voltage.

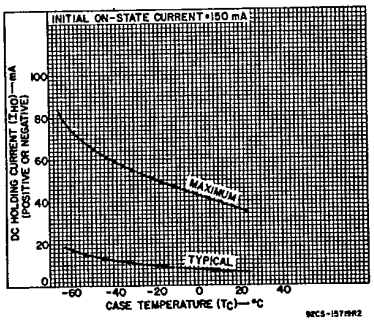


Fig. 8 - DC holding current (positive or negative) vs. case temperature.

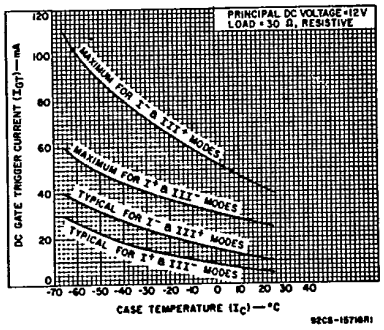


Fig. 9 - DC gate-trigger current vs. case temperature.

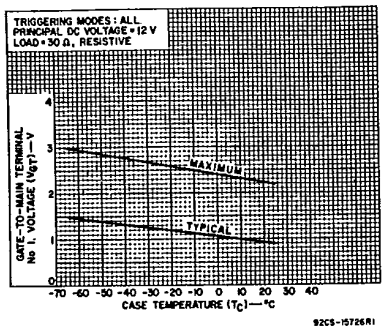


Fig. 10 - DC gate-trigger voltage vs. case temperature.