

N-Channel JFET Switch



2N4391 – 2N4393 / PN4391 – PN4393 / SST4391 – SST4393

FEATURES

- $r_{ds(on)} < 300 \text{ Ohms}$ (2N4391)
- $I_{D(OFF)} < 100 \text{ pA}$
- Switches $\pm 10 \text{ VAC}$ With $\pm 15 \text{ V}$ Supplies (4392, 4393)

PIN CONFIGURATION

TO-18

TO-92

5001

SOT-23

PRODUCT MARKING (SOT-23)	
SST4391	N01
SST4392	N02
SST4393	N03

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage -40V
Gate Current 10mA
Storage Temperature Range -65 $^{\circ}\text{C}$ to +200 $^{\circ}\text{C}$
Operating Temperature Range -55 $^{\circ}\text{C}$ to +200 $^{\circ}\text{C}$
Lead Temperature (Soldering, 10sec) +300 $^{\circ}\text{C}$

	TO-18	TO-92	SOT-23
Power Dissipation	1.8W	360mW	350mW
Derate above 25 $^{\circ}\text{C}$	10mW/ $^{\circ}\text{C}$	3.3mW/ $^{\circ}\text{C}$	2.8mW/ $^{\circ}\text{C}$
Plastic			
Storage			-55 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$
Operating			-55 $^{\circ}\text{C}$ to +135 $^{\circ}\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
2N4391/93	Hermetic TO-18	-55 $^{\circ}\text{C}$ to +200 $^{\circ}\text{C}$
PN4391/93	Plastic TO-92	-55 $^{\circ}\text{C}$ to +135 $^{\circ}\text{C}$
SST4391/93	Plastic SOT-23	-55 $^{\circ}\text{C}$ to +135 $^{\circ}\text{C}$
X2N4391/93	Sorted Chips in Carriers	-55 $^{\circ}\text{C}$ to +200 $^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

SYMBOL	PARAMETER	4391		4392		4393		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	$V_{GS} = -20\text{V}, V_{DS} = 0$ $T_A = 150^\circ\text{C}$
			-200		-200		-200	nA	
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\mu\text{A}, V_{DS} = 0$
$I_{D(off)}$	Drain Cutoff Current		100		100		100	pA	$V_{DS} = 20\text{V}$ $V_{GS} = -5\text{V}$ (4393) $V_{GS} = -7\text{V}$ (4392) $V_{GS} = -12\text{V}$ (4391) $T_A = 150^\circ\text{C}$
			200		200		200	nA	
$V_{GS(f)}$	Gate-Source Forward Voltage		1		1		1	V	$I_G = 1\text{mA}, V_{DS} = 0$
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3		$V_{DS} = 20\text{V}, I_D = 1\text{nA}$
I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	$V_{DS} = 20\text{V}, V_{GS} = 0$
$V_{DS(on)}$	Drain-Source ON Voltage		0.4		0.4		0.4	V	$V_{GS} = 0$ $I_D = 3\text{mA}$ (4393) $I_D = 6\text{mA}$ (4392) $I_D = 12\text{mA}$ (4391)
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0, I_D = 1\text{mA}$
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		$V_{GS} = 0, I_D = 0$ $f = 1\text{kHz}$
C_{iss}	Common-Source Input Capacitance (Note 2)		14		14		14	pF	$V_{DS} = 20\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)						3.5		$V_{DS} = 0$ $V_{GS} = -5\text{V}$ $V_{GS} = -7\text{V}$ $V_{GS} = -12\text{V}$
					3.5				
			3.5						
t_d	Turn-ON Delay Time (Note 2)		15		15		15	ns	$V_{DD} = 10\text{V}, V_{GS(on)} = 0$ $I_{D(on)} = 12\text{mA}$ $V_{GS(off)} = -12\text{V}$
t_r	Rise Time (Note 2)		5		5		5		
t_{off}	Turn-OFF Delay Time (Note 2)		20		35		50		
t_f	Fall Time (Note 2)		15		20		30		

NOTES: 1. Pulse test required, pulse width = 300 μs , duty cycle $\leq 3\%$.
2. For design reference only, not 100% tested.

SWITCHING TIMES TEST CIRCUIT

