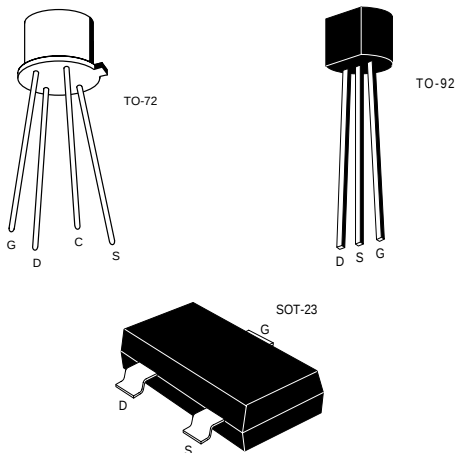


2N4117 – 2N4119 / 2N4117A – 2N4119A PN4117 – PN4119 / PN4117A – PN4119A / SST4117 – SST4119

PIN CONFIGURATION



5007

PRODUCT MARKING (SOT-23)

SST4117	T17
SST4118	T18
SST4119	T19

FEATURES

- Low Leakage
- Low Capacitance

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate-Source or Gate-Drain Voltage -40V
 Gate Current 50mA
 Storage Temperature Range -65°C to $+200^\circ\text{C}$
 Operating Temperature Range -55°C to $+175^\circ\text{C}$
 Lead Temperature (Soldering, 10sec) $+300^\circ\text{C}$
 Power Dissipation 300mW
 Derate above 25°C 2.0mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
2N4117-19/A	Hermetic TO-72	-55°C to $+175^\circ\text{C}$
PN4117-19/A	Plastic TO-92	-55°C to $+135^\circ\text{C}$
SST4117-19	Plastic SOT-23	-55°C to $+135^\circ\text{C}$
X2N4117-19/A	Sorted Chips in Carriers	-55°C to $+175^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

SYMBOL	PARAMETER	4117/A		4118/A		4119/A		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\mu\text{A}$, $V_{DS} = 0$
I_{GSS}	Gate Reverse Current		-10		-10		-10	pA	$V_{GS} = -20\text{V}$, $V_{DS} = 0$ $T_A = +150^\circ\text{C}$
		A devices	-1		-1		-1		
			-25		-25		-25	nA	
		A devices	-2.5		-2.5		-2.5		
$V_{GS(off)}$	Gate-Source Pinch-Off Voltage	-0.6	-1.8	-1	-3	-2	-6	V	$V_{DS} = 10\text{V}$, $I_D = 1\text{nA}$
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	0.02	0.09	0.08	0.24	0.20	0.60	mA	$V_{DS} = 10\text{V}$, $V_{GS} = 0$
g_{fs}	Common-Source Forward Transconductance (Note 1)	70	210	80	250	100	330	μS	$V_{DS} = 10\text{V}$, $f = 1\text{kHz}$
g_{fs}	Common-Source Forward Transconductance (Note 2)	60		70		90			$V_{GS} = 0$, $f = 30\text{MHz}$
g_{os}	Common-Source Output Conductance		3		5		10		$V_{DS} = 10\text{V}$, $V_{GS} = 0$, $f = 1\text{kHz}$
C_{iss}	Common-Source Input Capacitance (Note 2)		3		3		3	pF	$V_{DS} = 10\text{V}$, $V_{GS} = 0$, $f = 1\text{MHz}$
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)		1.5		1.5		1.5		$V_{DS} = 10\text{V}$, $V_{GS} = 0$, $f = 1\text{MHz}$

NOTES: 1. Pulse test: Pulse duration of 2ms used during test.
 2. For design reference only, not 100% tested.