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Philips Components–Signetics

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Memory Products	

27C64A

64K-bit CMOS EPROM (8K × 8)

DESCRIPTION

Philips Components–Signetics 27C64A CMOS EPROM is a 65,536-bit 5V read only memory organized as 8,192 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C64A has a non-multiplexed addressing interface and is configured in the JEDEC standard EPROM pinout.

Quick-pulse programming is employed on plastic devices which may speed up programming by as much as one hundred times. In the absence of quick-pulse programming equipment, the intelligent programming algorithm may be utilized.

The 27C64A is available in windowed Ceramic DIP, the Plastic DIP and the PLCC packages. This device can be programmed with standard EPROM programmers.

FEATURES

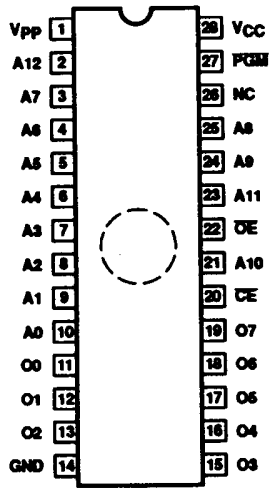
- Low power consumption
  - 100μA maximum CMOS standby current
- High-performance speed
  - 90ns maximum access time
- Noise immunity features
  - ±10% V_{CC} tolerance
  - Maximum latch-up immunity through Epitaxial processing
- Quick-pulse programming algorithm

PIN DESCRIPTION

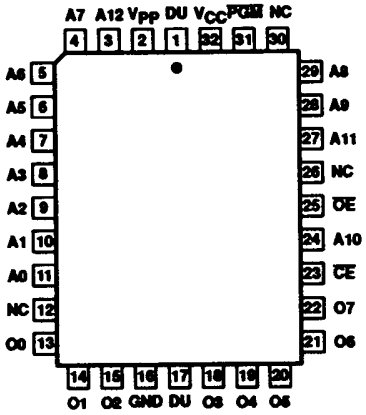
A0 - A12	Addresses
O0 - O7	Outputs
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
NC	No Connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
DU	Don't Use
$\overline{PGM}$	Program strobe

PIN CONFIGURATIONS

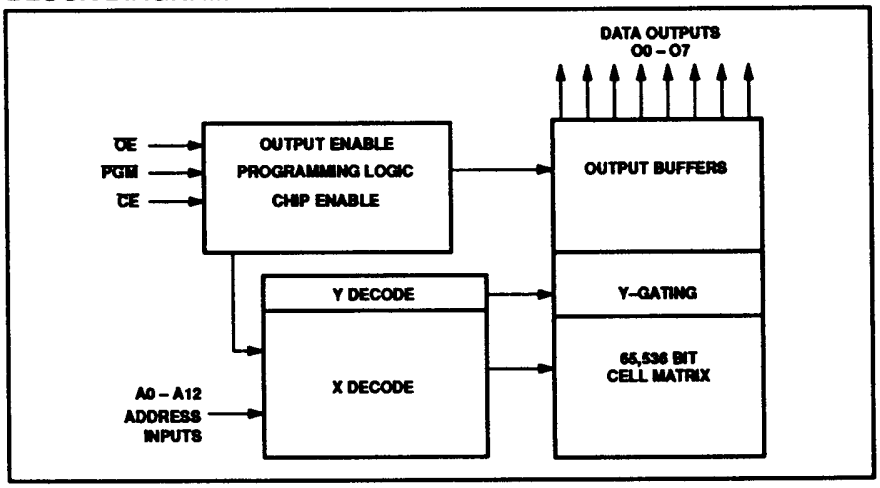
FA, N Packages



A Package



BLOCK DIAGRAM



Philips Components

PHILIPS

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64K-bit CMOS EPROM (8K × 8) 27C64A

READ MODE:

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C64A has a standby mode which reduces the maximum V_{CC} current to 100µA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE		
	COMMERCIAL	INDUSTRIAL	AUTOMOTIVE
28-Pin Ceramic Dual In-Line with quartz window 600mil-wide	27C64A-90 FA 27C64A-12 FA 27C64A-15 FA 27C64A-17 FA 27C64A-20 FA	27C64AI12 FA 27C64AI15 FA 27C64AI20 FA	27C64AA12 FA 27C64AA15 FA 27C64AA20 FA
28-Pin Plastic Dual In-Line 600mil-wide	27C64A-90 N 27C64A-12 N 27C64A-15 N 27C64A-17 N 27C64A-20 N	27C64AI12 N 27C64AI15 N 27C64AI20 N	27C64AA12 N 27C64AA15 N 27C64AA20 N
32-Pin Plastic Leaded Chip Carrier 450mil × 550mil	27C64A-90 A 27C64A-12 A 27C64A-15 A 27C64A-17 A 27C64A-20 A	27C64AI12 A 27C64AI15 A 27C64AI20 A	27C64AA12 A 27C64AA15 A 27C64AA20 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_{stg}	Storage temperature range	-65 to +125	°C
V_I, V_O	Voltage inputs and outputs	-2.0 to (V_{CC} + 1)	V
V_H	Voltage on A9[2] (During intelligent identifier interrogation)	-2.0 to +13.5	V
V_{PP}	Voltage on V_{PP} (During programming)	-2.0 to +14.0	V
V_{CC}	Supply voltage[2]	-2.0 to +7.0	V

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[1]

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}[2]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X[3]	X[3]	V_{CC}	Hi-Z

NOTES:

1. All voltages are with respect to network ground.
2. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
3. X can be V_{IH} or V_{IL}.

OPERATING TEMPERATURE RANGE

PARAMETER	RATING (°C)
Operating temperature range: T_{amb}	COMMERCIAL 0 to +70
	INDUSTRIAL -40 to +85
	AUTOMOTIVE -40 to +125

DC ELECTRICAL CHARACTERISTICS

Over operating temperature range, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[3]	MAX	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	-1.0	µA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			10	µA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$, $V_{OUT} = 5.5V = V_{CC}$	-1.0		1.0	µA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4, 6]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 11.1MHz $V_{PP} = V_{CC}$, O0 - O7 = 0mA			30	mA
I_{CC} CMOS	Operating (CMOS inputs)[4, 6]	$\overline{CE}$ = GND, f = 11.1MHz Inputs = V_{CC} or GND, I/O = 0mA			15	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	mA
I_{SB} CMOS	Standby (CMOS inputs)[5]	$\overline{CE} = V_{IH}$			100	µA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	-0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	-0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		V_{CC} + 0.5	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	V_{CC} - 0.2		V_{CC} + 0.2	V
V_{PP}	Read[8]	(Operating)	V_{CC} - 0.7		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	I_{OL} = 2.1mA			0.45	V
V_{OH}	High	I_{OH} = -2.5mA	3.5			V
Capacitance[9] T_{amb} = 25°C						
C_{IN}	Address and control	V_{CC} = 5.0V, f = 1.0MHz			6	pF
C_{OUT}	Outputs	V_{IN} = 0V, V_{OUT} = 0V			12	pF

NOTES:

1. Minimum DC input voltage is -0.5V. During transitions the inputs may undershoot to -2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at V_{CC} = 5V, T_{amb} = 25°C.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of I_{PP} + I_{CC} and is measured at a frequency of 11.1MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.

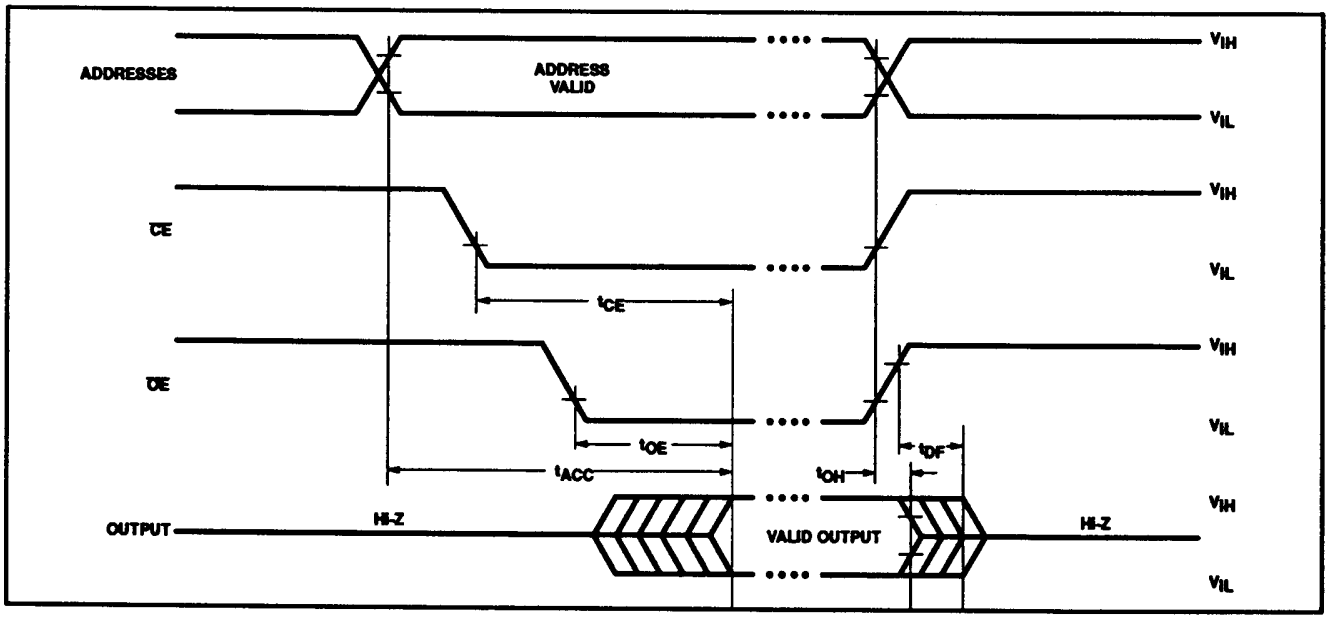
AC ELECTRICAL CHARACTERISTICS

Over operating temperature range, +4.5V ≤ V_{CC} ≤ +5.5V, R_L = 660Ω, C_L = 100pF[4]

SYMBOL	TO	FROM	27C64A-90		27C64A-12 27C64AI12 27C64AA12		27C64A-15 27C64AI15 27C64AA15		27C64A-17		27C64A-20 27C64AI20 27C64AA20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Access time[1]													
t_{ACC}	Output	Address		90		120		150		170		200	ns
t_{CE}	Output	$\overline{CE}$		90		120		150		170		200	ns
t_{OE}[3]	Output	$\overline{OE}$		40		60		65		70		75	ns
Disable time[2]													
t_{DF}	Output Hi-Z	$\overline{OE}$		25		30		45		50		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		0		0		0		ns

NOTES:
1. AC characteristics are tested at V_{IH} = 2.4V and V_{IL} = 0.45V. Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. For 90ns part, C_L = 30pF.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT

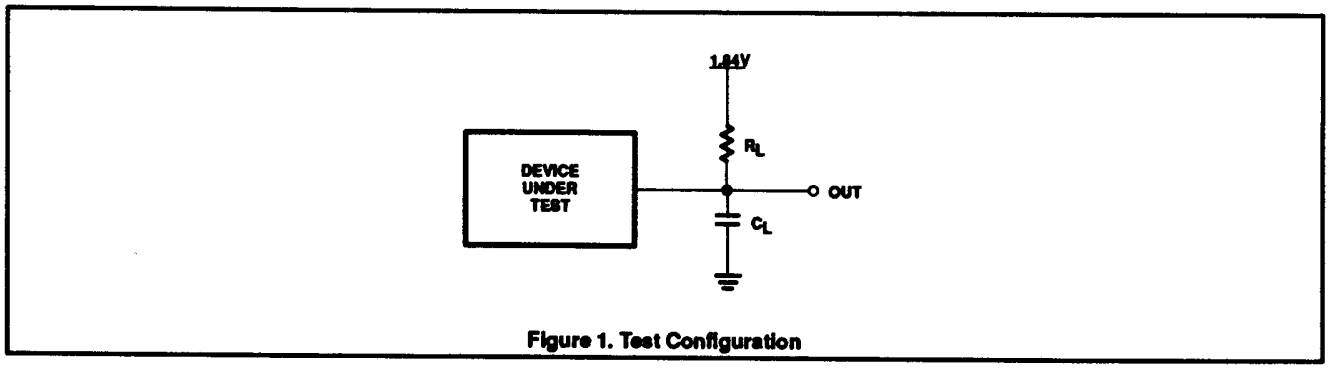


Figure 1. Test Configuration

PROGRAMMING INFORMATION

Complete programming system specifications for both the intelligent programming method and for the quick-pulse programming method are available upon request from Signetics Memory Marketing.

Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of EPROM programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers offering equipment certified by Signetics is available upon request from Signetics.

PROGRAMMING THE 27C64A

Caution: Exceeding 14.0V on V_{PP} Pin may permanently damage the 27C64A.

Initially, all bits of the 27C64A are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word.

The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

QUICK-PULSE PROGRAMMING ALGORITHM

Signetics plastic EPROMs can be programmed using the quick-pulse programming algorithm to substantially reduce the through-put time in the production environment. This algorithm typically allows plastic devices to be programmed in under four seconds, a significant improvement over previous algorithms. Actual programming time is a function of the EPROM programming equipment being used.

The quick-pulse programming algorithm uses initial pulses of 100µs followed by a byte verification to determine when the address byte has been successfully programmed. Up to 28 100µs pulses per byte are provided before a failure is recognized (refer to the following pages for algorithm specifications).

ERASURE CHARACTERISTICS

The erasure characteristics of the 27C64A are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 - 4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C64A in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C64A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 27C64A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The 27C64A should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C64A can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000µW/cm^2). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

INTELLIGENT PROGRAMMING ALGORITHM

The 27C64A intelligent programming algorithms rapidly program CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Actual programming times may vary due to differences in programming equipment.

The intelligent identifier also provides the reading out of a binary code from an EPROM that will identify its manufacturer and type. This is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25° ± 5°C ambient temperature range that is required when programming the 27C64A. To activate this mode, the programming equipment must force 11.5V to 12.5V on address A9 of the 27C64A. Two bytes may then be read from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. The $\overline{CE}$, $\overline{OE}$ and all other address lines must be at V_{IL} during interrogation.

The identifier information for Signetics 27C64A is as follows:

When A0 = V_{IL}	
data is "Manufacturer"	$15_{(HEX)}$
When A0 = V_{IH}	
data is "Product"	$0B_{(HEX)}$

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. The programming algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{PGM}$ pulse(s) is 1ms, which is then followed by a longer overprogram pulse of 3Xms. X is an iteration counter and is equal to the number of the initial 1ms pulses applied to a particular location before a correct verify occurs. Up to 25 1ms pulses per byte are provided for before the overprogram pulse is applied.

When the intelligent programming cycle has been completed, all bytes should be compared to the original data source with V_{CC} = 5.0V (refer to the following pages for algorithm specifications).

CMOS NOISE CHARACTERISTICS

Special epitaxial processing techniques have enabled Signetics to build CMOS with features that add to system reliability. These include input/output protection to latch-up for stresses up to 100mA on Address and Data pins that range from -1V to (V_{CC} + 1V). In addition, the V_{PP} (Programming) pin is designed to resist latch-up to the 14V maximum device limit.

SIGNETICS DISCOURAGES THE CONSTRUCTION AND USE OF "HOMEMADE" PROGRAMMING EQUIPMENT

In order to consistently achieve excellent programming yields, periodic calibration of the programming equipment is required. Consult the equipment manufacturer for the recommended calibration interval. Signetics warranty for programmability extends only to product that has been programmed on *certified* equipment that has been serviced to the manufacturers recommendation.

INTELLIGENT PROGRAMMING ALGORITHM

DC PROGRAMMING CHARACTERISTICS

T_{amb} = 25°C ±5°C, V_{CC} = 6.0V ±0.25V, V_{PP} = 12.5V ±0.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
I_I	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input low level (all inputs)		-0.1	0.8	V
V_{IH}	Input high level		2.4	6.5	V
V_{OL}	Output low voltage during verify	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output high voltage during verify	I_{OH} = -2.5mA	3.5		V
I_{CC2}	V_{CC} supply current	O0 - 15 = 0mA		50	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		50	mA

AC PROGRAMMING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP}[3]	$\overline{OE}$ high to output float delay		0		130	ns
t_{VPS}	V_{PP} setup time		2			µs
t_{VCS}	V_{CC} setup time		2			µs
t_{CES}	$\overline{CE}$ setup time		2			µs
t_{PW}	$\overline{CE}$ initial program pulse width	Note 1	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width	Note 2	2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	µs

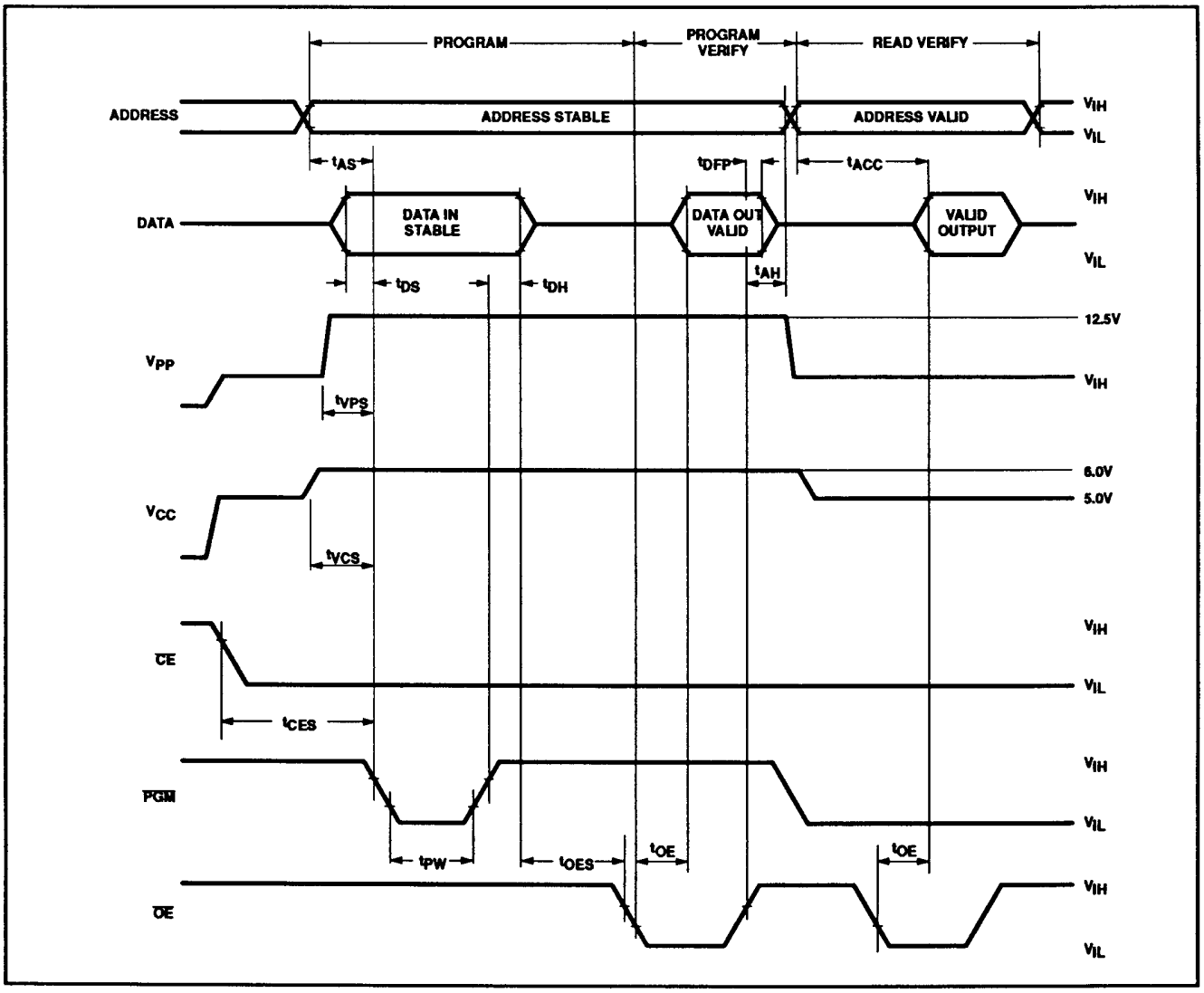
AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

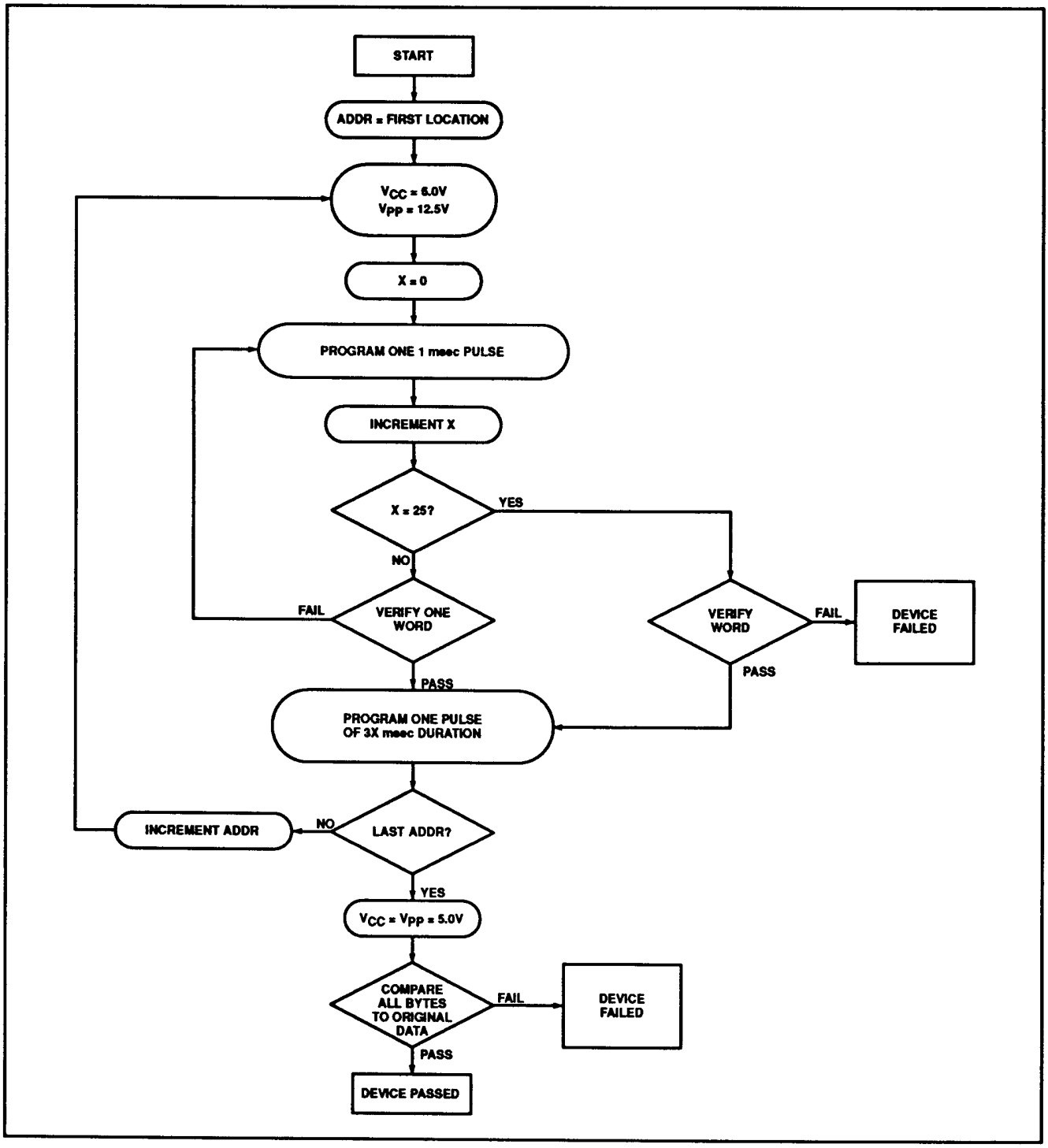
NOTES:

1. Initial program pulse width tolerance is 1ms ±5%.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of iteration counter value X.
3. The parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
4. During programming, a 0.1µf capacitor is required from V_{PP} to GND node, to suppress voltage transients that can damage the device.

INTELLIGENT PROGRAMMING ALGORITHM WAVEFORMS



INTELLIGENT PROGRAMMING ALGORITHM FLOWCHART



QUICK PULSE PROGRAMMING ALGORITHM

DC PROGRAMMING CHARACTERISTICS

T_{amb} = 25°C ±5°C, V_{CC} = 6.25V ±0.25V, V_{PP} = 12.75V ±0.25V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
I_I	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input low level (all inputs)		-0.1	0.8	V
V_{IH}	Input high level		2.4	6.5	V
V_{OL}	Output low voltage during verify	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output high voltage during verify	I_{OH} = -2.5mA	3.5		V
I_{CC2}	V_{CC} supply current	O0 - 15 = 0mA		50	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		50	mA
V_{PP}	Programming voltage		12.5	13.0	V

AC PROGRAMMING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP}[3]	$\overline{OE}$ high to output float delay		0		130	ns
t_{VPS}	V_{PP} setup time		2			µs
t_{VCS}	V_{CC} setup time		2			µs
t_{PW}	$\overline{CE}$ initial program pulse width	Note 1	.095	0.100	0.105	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width	Note 2	2.85		78.8	ms
t_{OE}	Data valid from $\overline{OE}$				150	µs

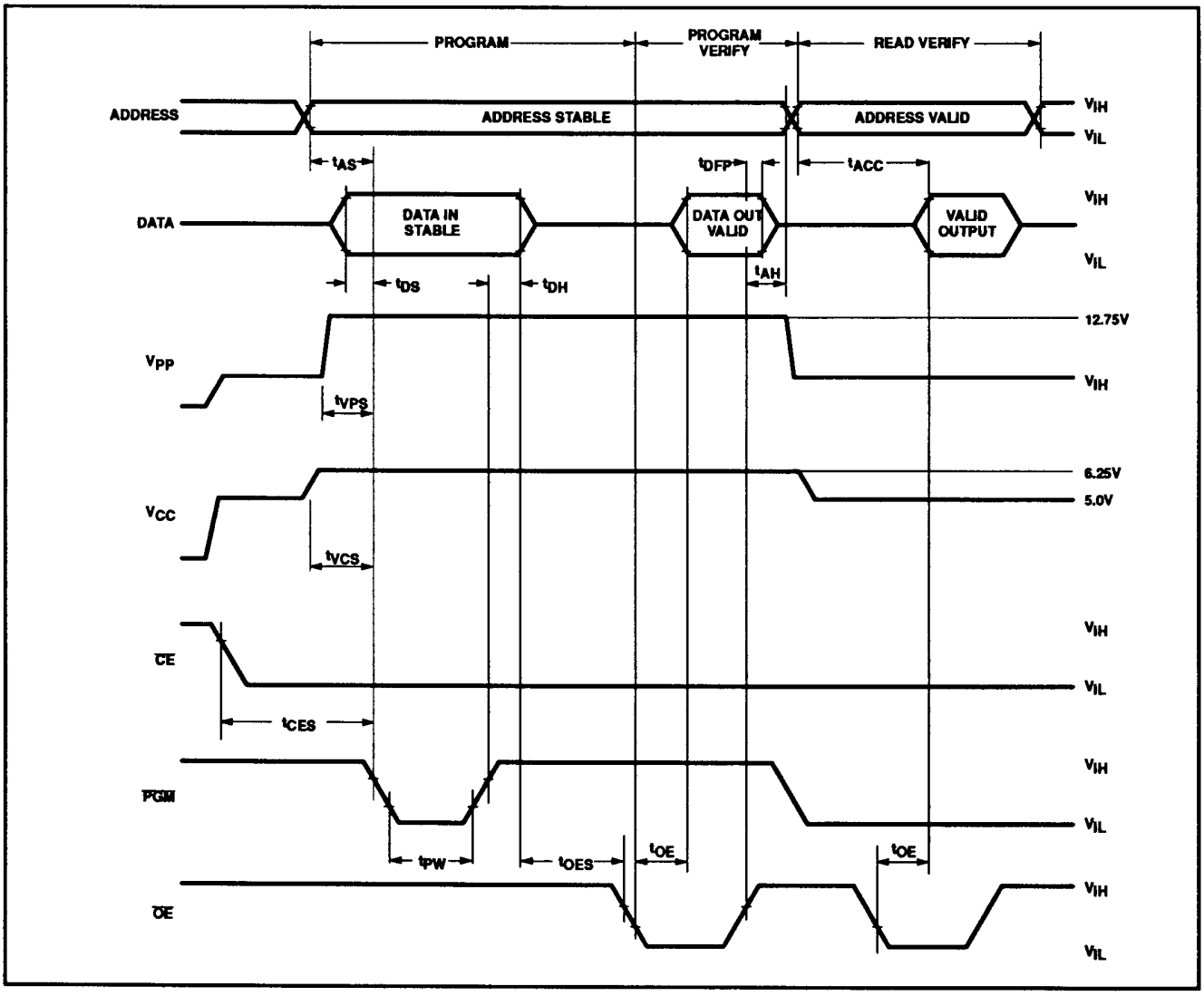
AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

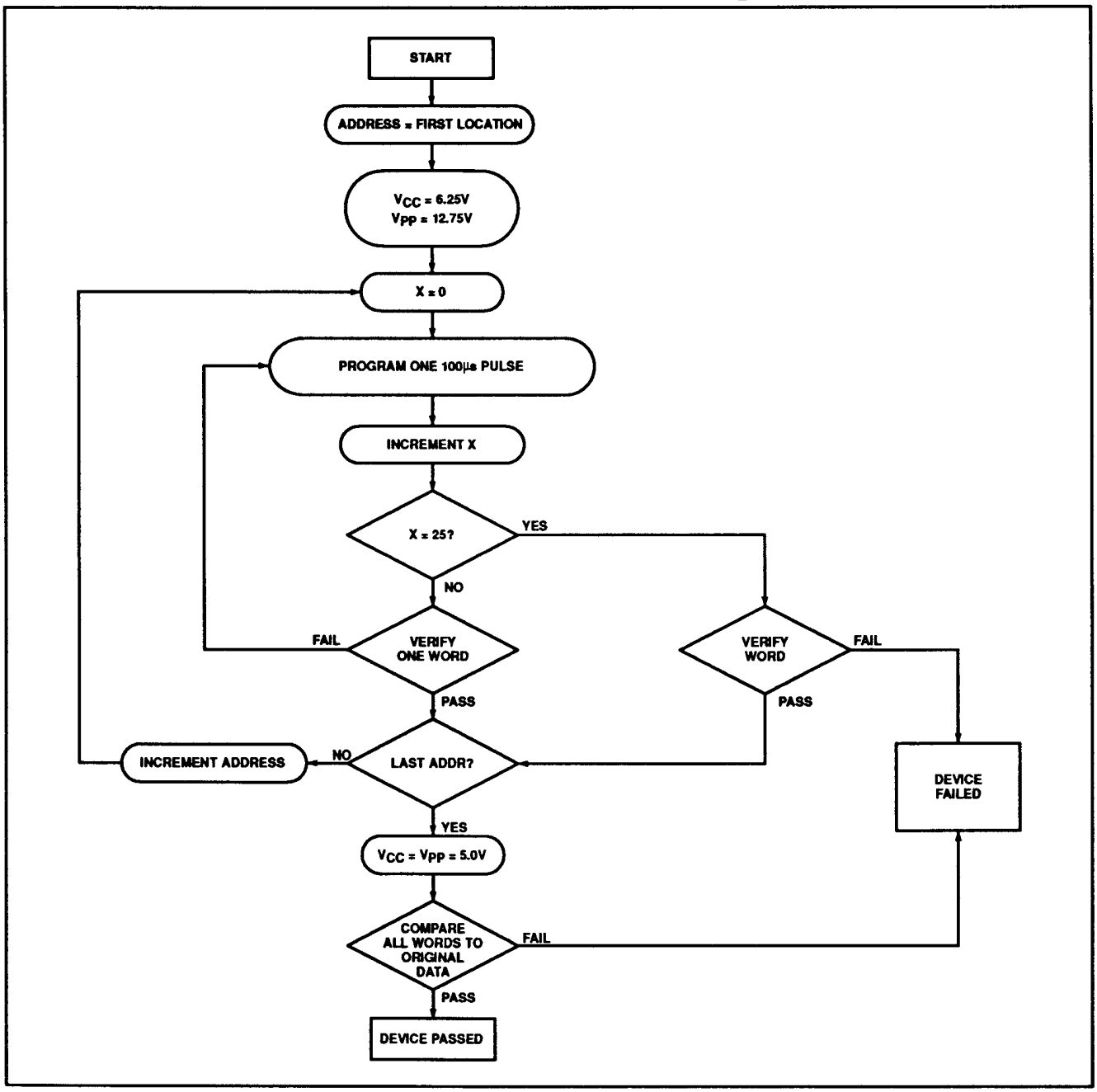
NOTES:

1. Initial program pulse width tolerance is 1ms ±5%.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of iteration counter value X.
3. The parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
4. During programming, a 0.1µf capacitor is required from V_{PP} to GND node, to suppress voltage transients that can damage the device.

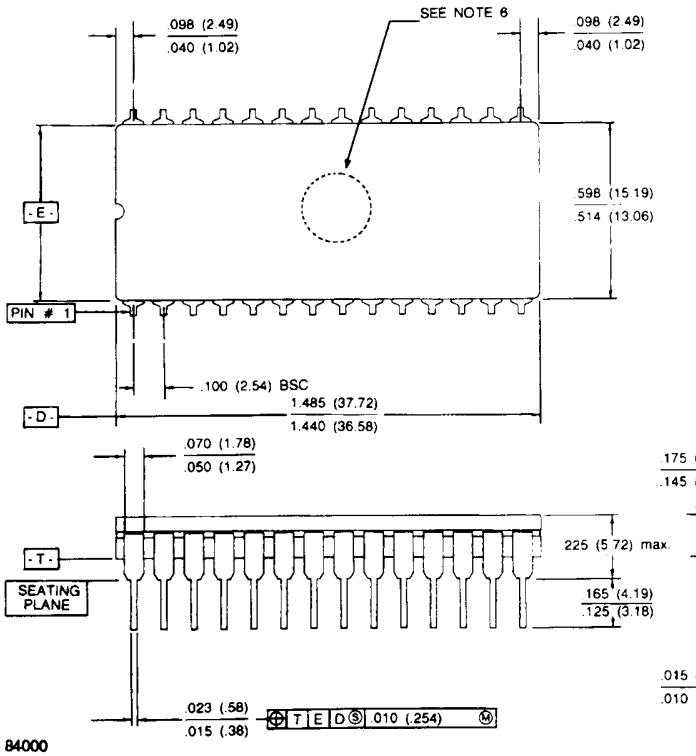
QUICK PULSE PROGRAMMING ALGORITHM WAVEFORMS



QUICK PULSE PROGRAMMING ALGORITHM FLOWCHART



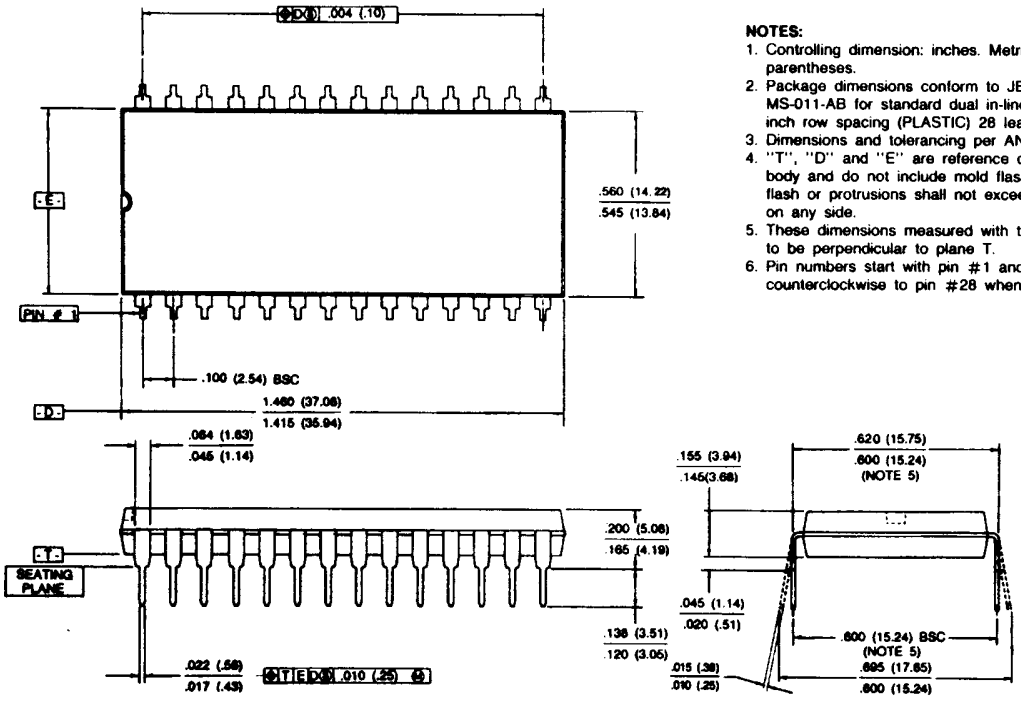
28-PIN (600 mils wide) CERAMIC DUAL IN-LINE WITH WINDOW (F) PACKAGE



NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.
6. Denotes window location for EPROM products (see FA package).

853-0589 84000 FQ3

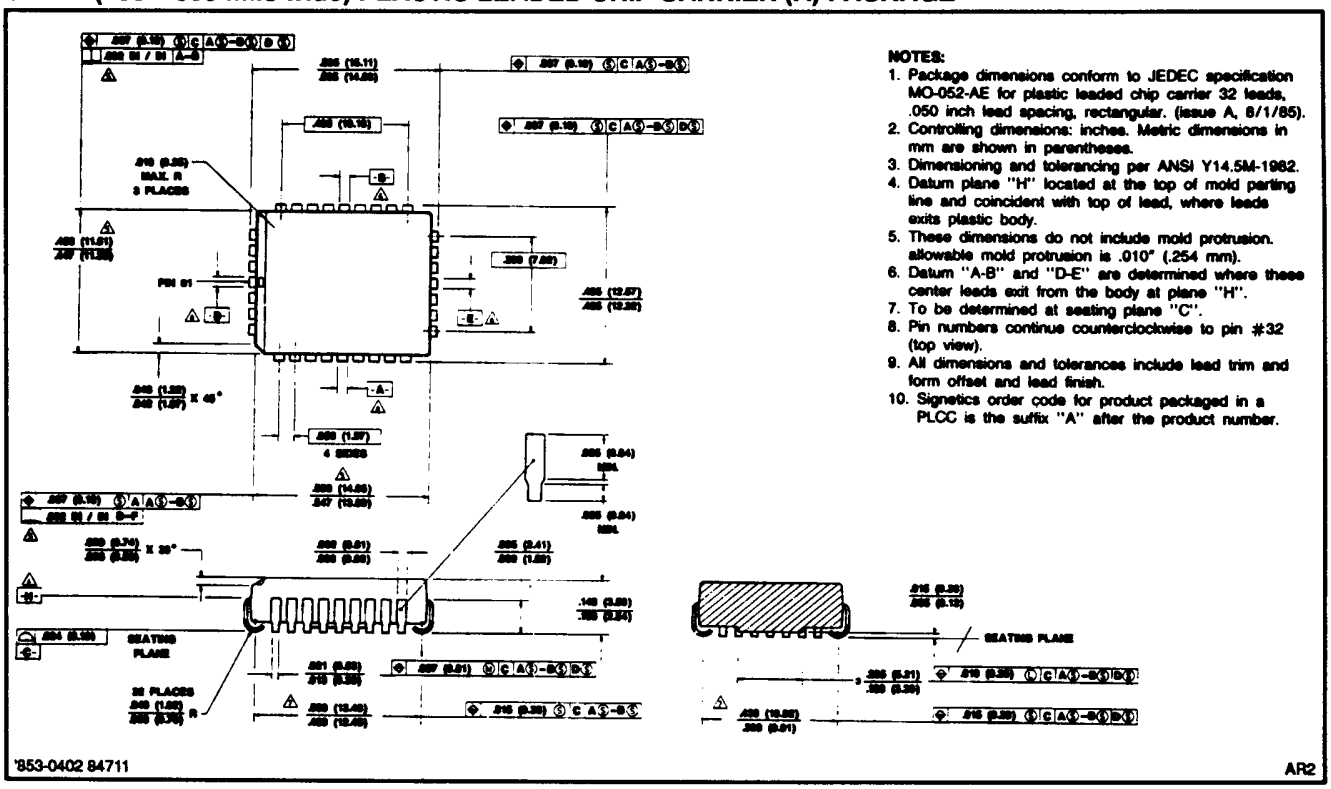
28-PIN (600 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

853-0413 84099 NQ3

32-PIN (450 × 550 mils wide) PLASTIC LEADED CHIP CARRIER (A) PACKAGE



NOTES:
1. Package dimensions conform to JEDEC specification MO-052-AE for plastic leaded chip carrier 32 leads, .050 inch lead spacing, rectangular. (issue A, 8/1/85).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where leads exits plastic body.
5. These dimensions do not include mold protrusion. allowable mold protrusion is .010" (.254 mm).
6. Datum "A-B" and "D-E" are determined where these center leads exit from the body at plane "H".
7. To be determined at seating plane "C".
8. Pin numbers continue counterclockwise to pin #32 (top view).
9. All dimensions and tolerances include lead trim and form offset and lead finish.
10. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.

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64K-bit CMOS EPROM (8K × 8) 27C64A

DEFINITIONS

Data Sheet Identification	Product Status	Definition
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