Obsolete Device

27C64

64K (8K x 8) CMOS EPROM

FEATURES

- High speed performance
  - 120 ns access time available
- CMOS Technology for low power consumption
  - 20 mA Active current
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed “express” programming algorithm
- Organized 8K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
  - Tape and reel
- Available for the following temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

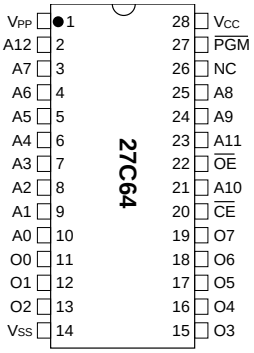
DESCRIPTION

The Microchip Technology Inc. 27C64 is a CMOS 64K bit (electrically) Programmable Read Only Memory. The device is organized as 8K words by 8 bits (8K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120 ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.

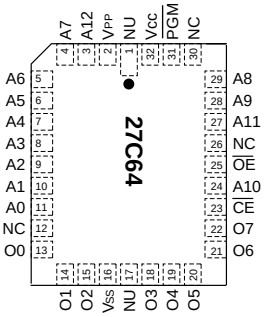
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES

DIP/SOIC



PLCC



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC} and input voltages w.r.t. V_{SS} ..... -0.6V to + 7.25V

V_{PP} voltage w.r.t. V_{SS} during programming ..... -0.6V to +14V

Voltage on A9 w.r.t. V_{SS} ..... -0.6V to +13.5V

Output voltage w.r.t. V_{SS} .....-0.6V to V_{CC} +1.0V

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied .....-65°C to +125°C

*Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
V_{PP}	Programming Voltage
O0 - O7	Data Output
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

V_{CC} = +5V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.5	V_{CC}+1 0.8	V V	
Input Leakage	all	—	I_{LI}	-10	10	µA	V_{IN} = 0 to V_{CC}
Output Voltages	all	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
Output Leakage	all	—	I_{LO}	-10	10	µA	V_{OUT} = 0V to V_{CC}
Input Capacitance	all	—	C_{IN}	—	6	pF	V_{IN} = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	C_{OUT}	—	12	pF	V_{OUT} = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I	TTL input TTL input	I_{CC1} I_{CC2}	— —	20 25	mA mA	V_{CC} = 5.5V; V_{PP} = V_{CC}; f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = V_{IL}; I_{OUT} = 0 mA; V_{IL} = -0.1 to 0.8V; V_{IH} = 2.0 to V_{CC}; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	$I_{CC(S)}$ — —	— — —	2 3 100	mA mA µA	 $\overline{CE}$ = V_{CC} ± 0.2V
I_{PP} Read Current V_{PP} Read Voltage	all all	Read Mode Read Mode	I_{PP} V_{PP}	 V_{CC}-0.7	100 V_{CC}	µA V	V_{PP} = 5.5V

* Parts: C=Commercial Temperature Range; I =Industrial Temperature Range.

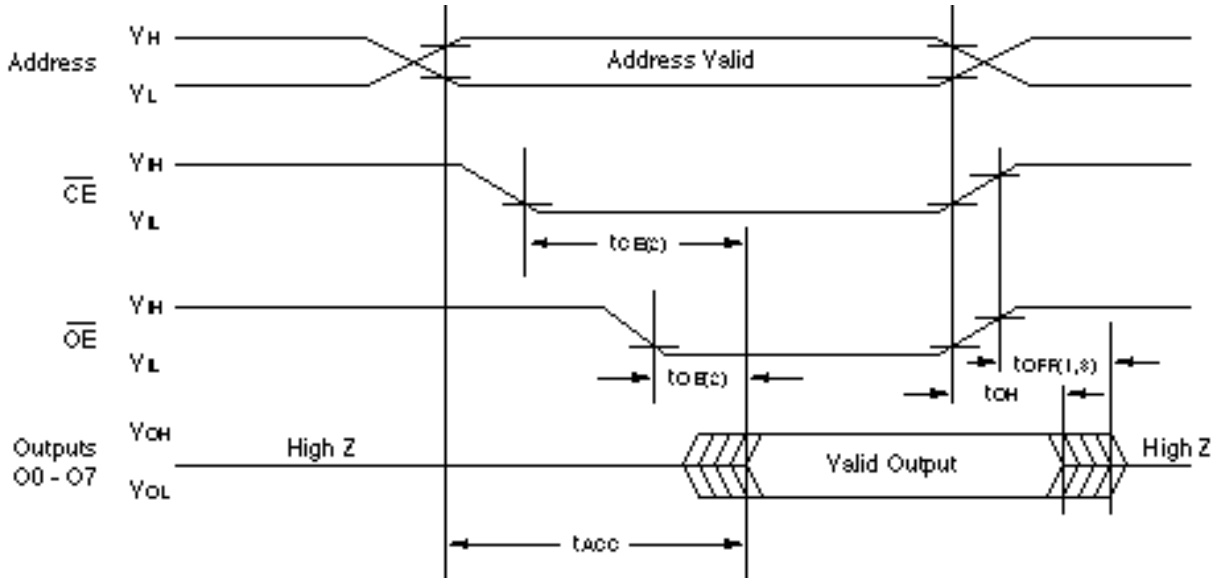
Note 1: Typical active current increases .5 mA per MHz up to operating frequency for all temperature ranges.

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TABLE 1-3: READ OPERATION AC CHARACTERISTICS

	AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C												
Parameter	**Sym**	**27C64-12**		**27C64-15**		**27C64-17**		**27C64-20**		**27C64-25**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	t_{ACC}	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	65	—	70	—	70	—	75	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t_{OH}	0	—	0	—	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Note 1: tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
2: $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE.
3: This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic"1" Logic"0"	V_{OH} V_{OL}	2.4 —	— 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
V_{CC} Current, program & verify	—	I_{CC2}	—	20	mA	Note 1
V_{PP} Current, program	—	I_{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

Note 1: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

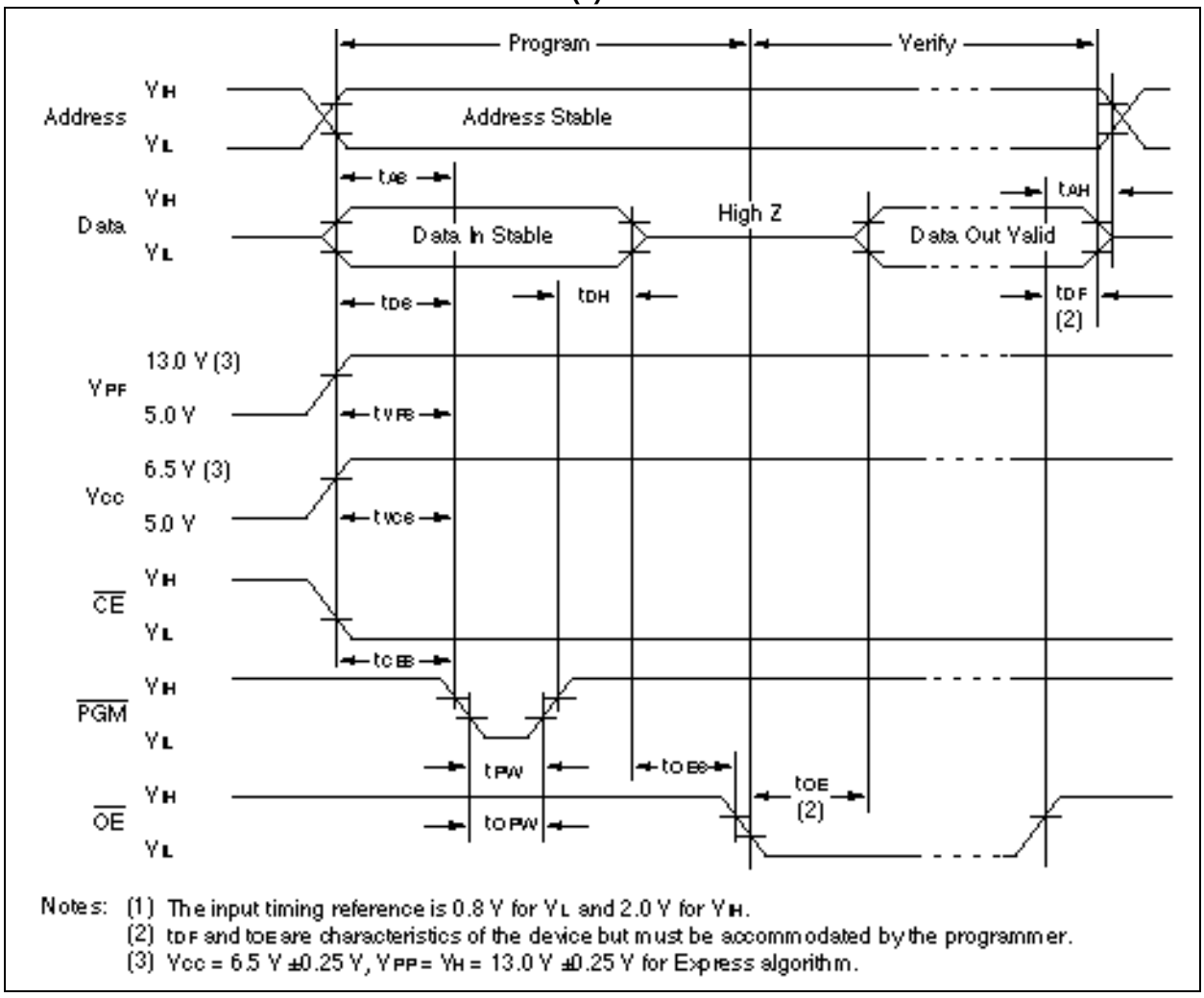
for Program, Program Verify and Program Inhibit Modes		AC Testing Waveform: V_{IH}=2.4V and V_{IL}=0.45V; V_{OH}=2.0V; V_{OL}=0.8V Ambient Temperature: Tamb=25°C ±5°C V_{CC}= 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.

2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

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FIGURE 1-2: PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference is 0.8 V for VL and 2.0 V for VH.
(2) tDF and tOE are characteristics of the device but must be accommodated by the programmer.
(3) VCC = 6.5 V ±0.25 V, VPP = VH = 13.0 V ±0.25 V for Express algorithm.

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

1.4 Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

a) V_{CC} is brought to the proper voltage,
b) V_{PP} is brought to the proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

1.9 Identity Mode

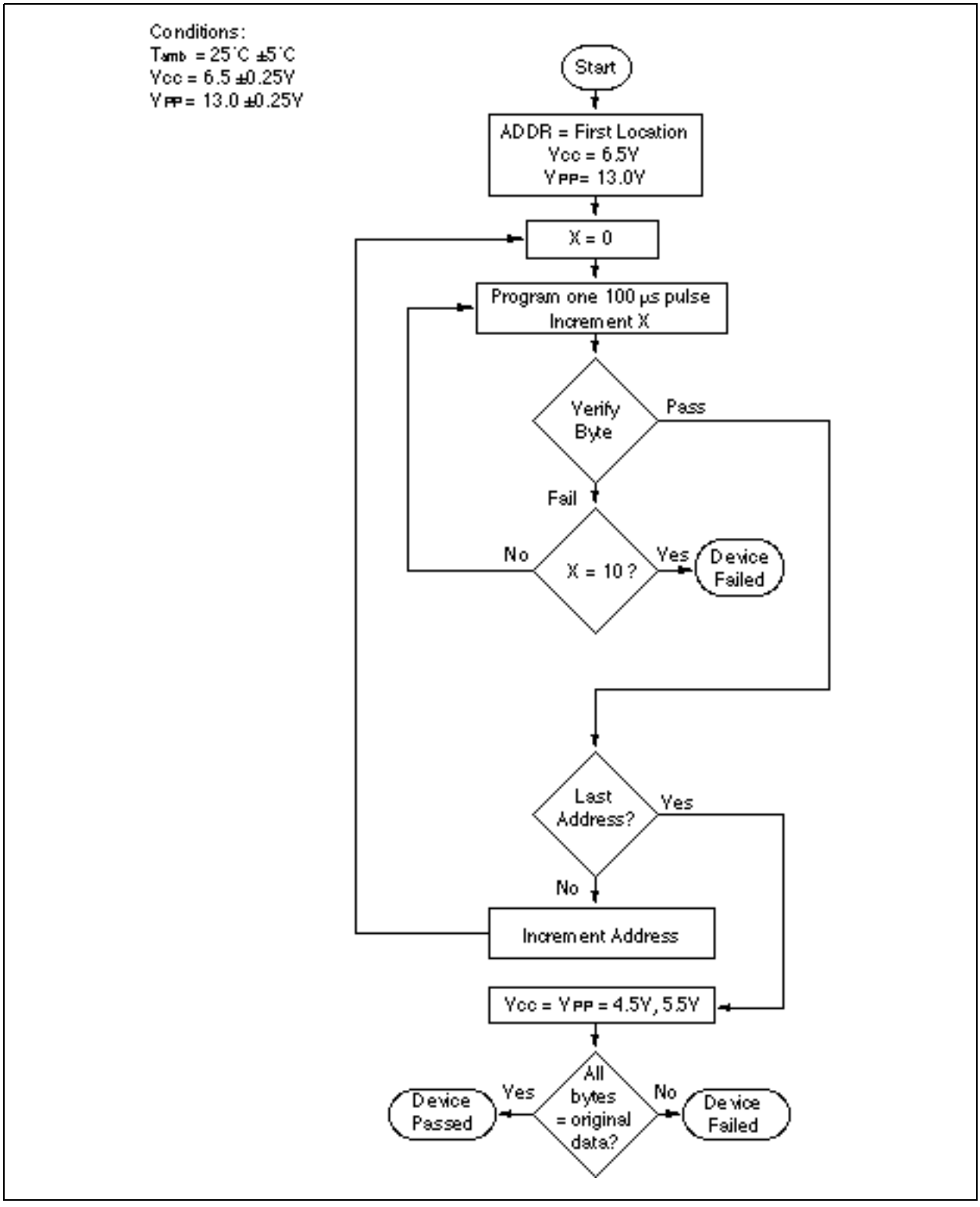
In this mode, specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	**Input**	**Output**								
Identity ↓	**A0**	**O7**	**O6**	**O5**	**O4**	**O3**	**O2**	**O1**	**O0**	**Hex**
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	0	0	0	0	0	0	1	0	02

* Code subject to change

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FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C64 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27C64 – 25 I /P

Package:	L	=	Plastic Leaded Chip Carrier
	P	=	Plastic DIP (600 Mil)
	SO	=	Plastic SOIC (300 Mil)
Temperature Range:	Blank	=	0°C to +70°C
	I	=	–40°C to +85°C
Access Time:	12	=	120 ns
	15	=	150 ns
	17	=	170 ns
	20	=	200 ns
	25	=	250 ns
Device:	27C64		64K (8K x 8) CMOS EPROM

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