24LC22A

2K VESA® E-EDID™ Serial EEPROM

Features:

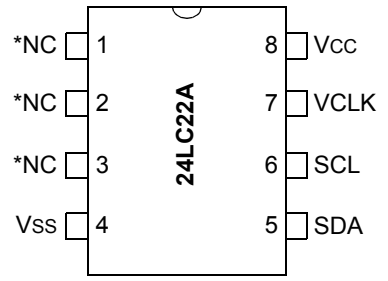
- Single Supply with Operation Down to 2.5V
- Supports Enhanced EDID™ (E-EDID™) 1.3
- Completely Implements DDC1™/DDC2™ Interface for Monitor Identification, Including Recovery to DDC1
- 2 Kbit Serial EEPROM Low-Power CMOS Technology:
  - 1 mA typical active current
  - 10 uA standby current typical at 5.5V
- 2-Wire Serial Interface Bus, I^2C™ Compatible
- 100 kHz (2.5V) and 400 kHz (5V) Compatibility
- Self-Timed Write Cycle (including Auto-Erase)
- Page-Write Buffer for up to Eight Bytes
- 1,000,000 Erase/Write Cycles
- Data Retention >200 years
- ESD Protection >4000V
- 8-pin PDIP and SOIC Packages
- Available Temperature Ranges:
  - Industrial (I) -40°C to +85°C
- Pb-Free and RoHS Compliant

Description:

The Microchip Technology Inc. 24LC22A is a 256 x 8-bit dual-mode Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: Transmit-Only mode (1 Kbit) and Bidirectional mode (2 Kbit). Upon power-up, the device will be in the Transmit-Only mode, sending a serial bit stream of the memory array from 00h to 7Fh, clocked by the VCLK pin. A valid high-to-low transition on the SCL pin will cause the device to enter the Transition mode, and look for a valid control byte on the I^2C bus. If it detects a valid control byte from the master, it will switch into Bidirectional mode, with byte selectable read/write capability of the entire 2K memory array using SCL. If no control byte is received, the device will revert to the Transmit-Only mode after it receives 128 consecutive VCLK pulses while the SCL pin is idle. The 24LC22A is available in standard 8-pin PDIP and SOIC packages.

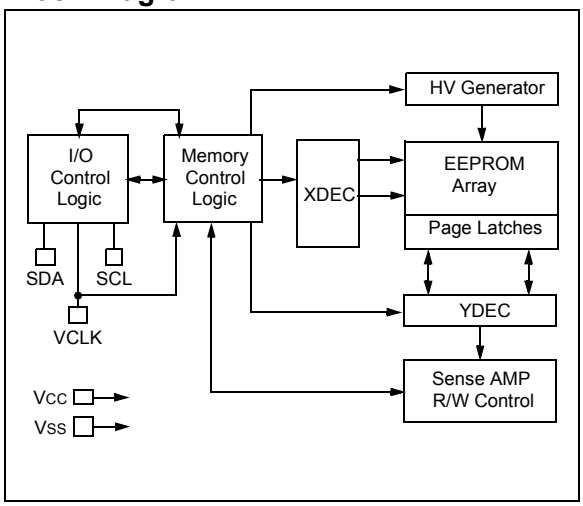
Package Types

PDIP/SOIC



* Pins labeled 'NC' has no internal connections

Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{CC}.....7.0V

All inputs and outputs w.r.t. V_{SS} ..... -0.6V to V_{CC} +1.0V

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied .....-40°C to +125°C

Soldering temperature of leads (10 seconds) .....+240°C

ESD protection on all pins .....≥ 4 kV

†Notice: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 DC Characteristics

DS CHARACTERISTICS			Vcc = +2.5V to 5.5V Industrial (I): T_{AMB} = -40°C to +85°C			
Param. No.	**Sym**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
SCL and SDA pins:						
D1	V_{IH}	High-level input voltage	0.7 V_{CC}	—	V	
D2	V_{IL}	Low-level input voltage	—	0.3 V_{CC}	V	
Input levels on VCLK pin:						
D3	V_{IH}	High-level input voltage	2.0	—	V	$V_{CC} \geq$ 2.7V **(Note)**
D4	V_{IL}	Low-level input voltage	—	0.2 V_{CC}	V	$V_{CC} \leq$ 2.7V **(Note)**
D5	V_{HYS}	Hysteresis of Schmitt trigger Inputs	.05 V_{CC}	—	V	**(Note)**
D6	$V_{OL}1$	Low-level output voltage	—	0.4	V	I_{OL} = 3 mA, V_{CC} = 2.5V **(Note)**
D7	$V_{OL}2$	Low-level output voltage	—	0.6	V	I_{OL} = 6 mA, V_{CC} = 2.5V
D8	I_{LI}	Input leakage current	-10	10	µA	V_{IN} = V_{SS} or V_{CC}
D9	I_{LO}	Output leakage current	-10	10	µA	V_{OUT} = V_{SS} or V_{CC}
D10	C_{IN}, C_{OUT}	Pin capacitance (all inputs/outputs)	—	10	pF	V_{CC} = 5.0V **(Note)** T_{AMB} = 25°C, F_{CLK} = 1 MHz
Operating current:						
D10	I_{CC} WRITE	Operating current	—	3	mA	V_{CC} = 5.5V,
D11	I_{CC} READ	Operating current	—	1	mA	V_{CC} = 5.5V, SCL = 400 kHz
D12	I_{CCS}	Standby current	— —	30 100	µA µA	V_{CC} = 3.0V, SDA = SCL = V_{CC} V_{CC} = 5.5V, SDA = SCL = V_{CC} V_{CLK} = V_{SS}

Note: This parameter is periodically sampled and not 100% tested.

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1.2 AC Characteristics

AC CHARACTERISTICS			Vcc = +2.5V to 5.5V Industrial (I): TAMB = -40°C to +85°C			
Param. No.	**Sym.**	**Parameter**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock frequency	— —	100 400	kHz	2.5V ≤ VCC ≤ 5.5V 4.5V ≤ VCC ≤ 5.5V
2	THIGH	Clock high time	4000 600	— —	ns	2.5V ≤ VCC ≤ 5.5V 4.5V ≤ VCC ≤ 5.5V
3	TLOW	Clock low time	4700 1300	— —	ns	2.5V ≤ VCC ≤ 5.5V 4.5V ≤ VCC ≤ 5.5V
4	TR	SDA and SCL rise time	— —	1000 300	ns	2.5V ≤ VCC ≤ 5.5V (**Note 1**) 4.5V ≤ VCC ≤ 5.5V (**Note 1**)
5	TF	SDA and SCL fall time	— —	300 300	ns	(**Note 1**)
6	THD:STA	Start condition hold time	4000 600	— —	ns	2.5V ≤ VCC ≤ 5.5V 4.5V ≤ VCC ≤ 5.5V
7	TSU:STA	Start condition setup time	4700 600	— —	ns	2.5V ≤ VCC ≤ 5.5V 4.5V ≤ VCC ≤ 5.5V
8	THD:DAT	Data input hold time	0 0	— —	ns	(**Note 2**)
9	TSU:DAT	Data input setup time	250 100	— —	ns	2.5V ≤ VCC ≤ 5.5V 4.5V ≤ VCC ≤ 5.5V
10	TSU:STO	Stop condition setup time	4000 600	— —	ns	2.5V ≤ VCC ≤ 5.5V 4.5V ≤ VCC ≤ 5.5V
11	TAA	Output valid from clock (Note 2)	— —	3500 900	ns	2.5V ≤ VCC ≤ 5.5V 4.5V ≤ VCC ≤ 5.5V
12	TBUF	Bus free time: Time the bus must be free before a new transmission can start	4700 1300	— —	ns	2.5V ≤ VCC ≤ 5.5V 4.5V ≤ VCC ≤ 5.5V
13	TOF	Output fall time from VIH minimum to VIL maximum	— 20+0.1CB	250 250	ns	2.5V ≤ VCC ≤ 5.5V (**Note 1**) 4.5V ≤ VCC ≤ 5.5V (**Note 1**)
14	TSP	Input filter spike suppression (SDA and SCL pins)	— —	50 50	ns	(**Notes 1 and 3**)
15	TWR	Write cycle time (byte or page)	— —	10 10	ms	
16	TVAA	Output valid from VCLK	— —	2000 1000	ns	
17	TVHIGH	VCLK high time	4000 600	— —	ns	
18	TVLOW	VCLK low time	4700 1300	— —	ns	
19	TVHST	VCLK setup time	0 0	— —	ns	
20	TSPVL	VCLK hold time	4000 600	— —	ns	
21	TVHZ	Mode transition time	— —	1000 500	ns	
22	TVPU	Transmit-Only power up time	0 0	— —	ns	
23	TSPV	Input filter spike suppression (VCLK pin)	— —	100 100	ns	
24	—	Endurance	1M	—	cycles	25°C, VCC = 5.0V, Block mode (**Note 4**)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but established by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

2.0 FUNCTIONAL DESCRIPTION

The 24LC22A is designed to comply to the DDC Standard proposed by VESA (Figure 3-3) with the exception that it is not Access.bus capable. It operates in two modes, the Transmit-Only mode (1 Kbit) and the Bidirectional mode (2 Kbit). There is a separate 2-wire protocol to support each mode, each having a separate clock input but sharing a common data line (SDA). The device enters the Transmit-Only mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high-to-low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the Bidirectional mode and look for its control byte to be sent by the master. If it detects its control byte, it will stay in the Bidirectional mode. Otherwise, it will revert to the Transmit-Only mode after it sees 128 VCLK pulses.

2.1 Transmit-Only Mode

The device will power-up in the Transmit-Only mode at address 00h. This mode supports a unidirectional 2-wire protocol for continuous transmission of the first 1 Kbit of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only mode (Section 2.2). In this mode, data is transmitted on the SDA pin in 8-bit bytes, with each byte followed by a ninth, Null bit (Figure 2-1). The clock source for the Transmit-Only mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted Most Significant bit first. Each byte within the memory array will be output in sequence. After address 7Fh in the memory array is transmitted, the internal Address Pointers will wrap-around to the first memory location (00h) and continue. The Bidirectional mode Clock (SCL) pin must be held high for the device to remain in the Transmit-Only mode.

2.2 Initialization Procedure

After VCC has stabilized, the device will be in the Transmit-Only mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal sychronization. During this period, the SDA pin will be in a high-impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the Most Significant bit in address 00h. (Figure 2-2).

FIGURE 2-1: TRANSMIT-ONLY MODE

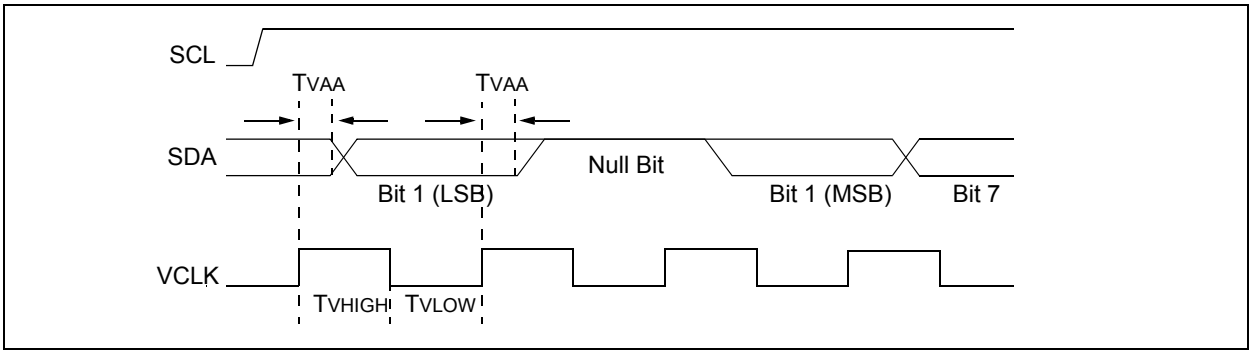
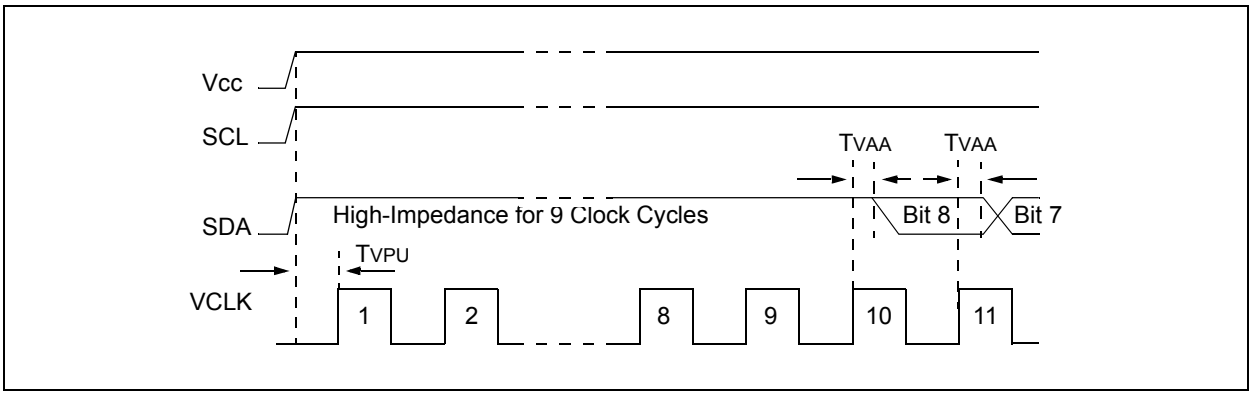


FIGURE 2-2: DEVICE INITIALIZATION



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3.0 BIDIRECTIONAL MODE

Before the 24LC22A can be switched into the Bidirectional mode (Figure 3-1), it must enter the Transition mode, which is done by applying a valid high-to-low transition on the Bidirectional mode clock (SCL). As soon it enters the Transition mode, it looks for a control byte '1010 000X' on the I²C™ bus, and starts to count pulses on VCLK. Any high-to-low transition on the SCL line will reset the count. If it sees a pulse count of 128 on VCLK while the SCL line is idle, it will revert back to the Transmit-Only mode, and transmit its contents starting with the Most Significant bit in address 00h. However, if it detects the control byte on the I²C bus, (Figure 3-2) it will switch to the in the Bidirectional mode. Once the device has made the transition to the Bidirectional mode, the only way to switch the device back to the Transmit-Only mode is to remove power from the device. The mode transition process is shown in detail in Figure 3-3.

Once the device has switched into the Bidirectional mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. In Bidirectional mode the user has access to the entire 2K array, whereas in the Transmit-Only mode the user can only access the first 1K. This mode supports a two-wire Bidirectional data transmission protocol (I²C). In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bidirectional mode clock (SCL), controls access to the bus and generates the Start and Stop conditions, while the 24LC22A acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. In the Bidirectional mode, the 24LC22A only responds to commands for device '1010 000X'.

FIGURE 3-1: MODE TRANSITION WITH RECOVERY TO TRANSMIT-ONLY MODE

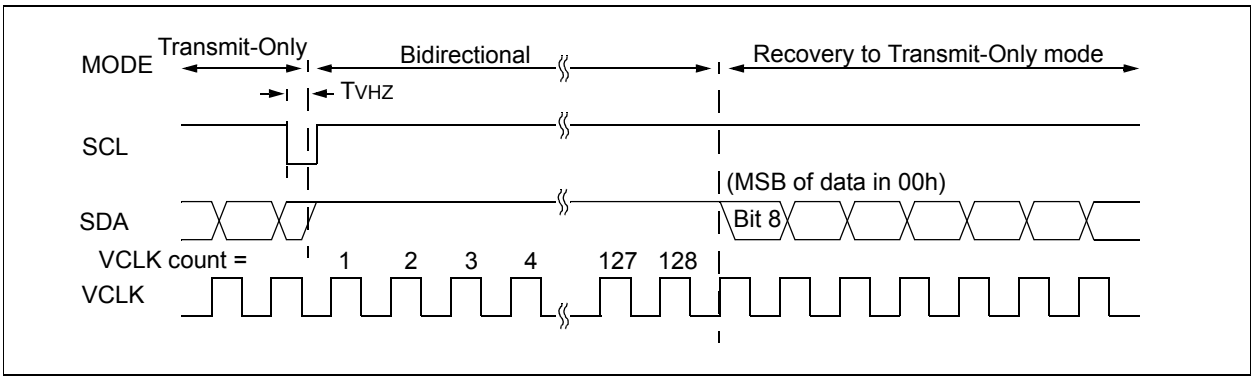


FIGURE 3-2: SUCCESSFUL MODE TRANSITION TO BIDIRECTIONAL MODE

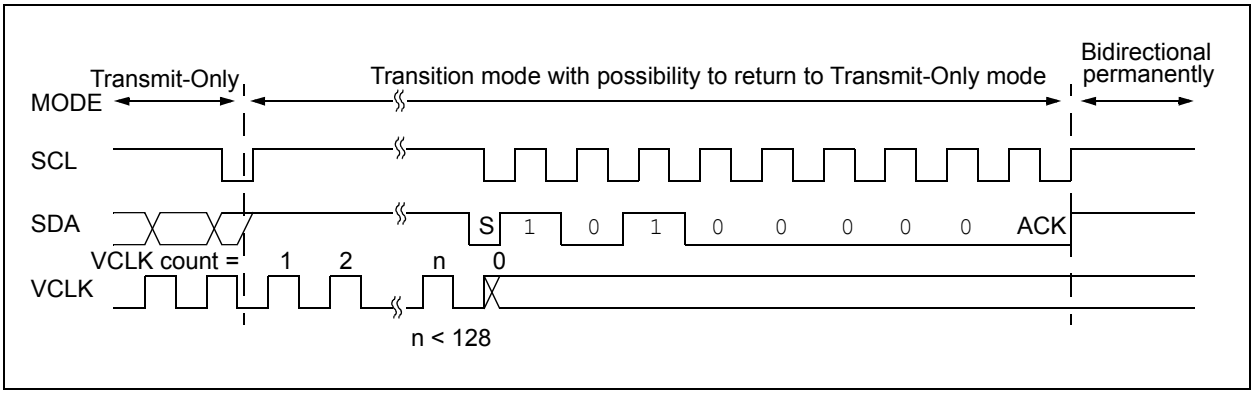
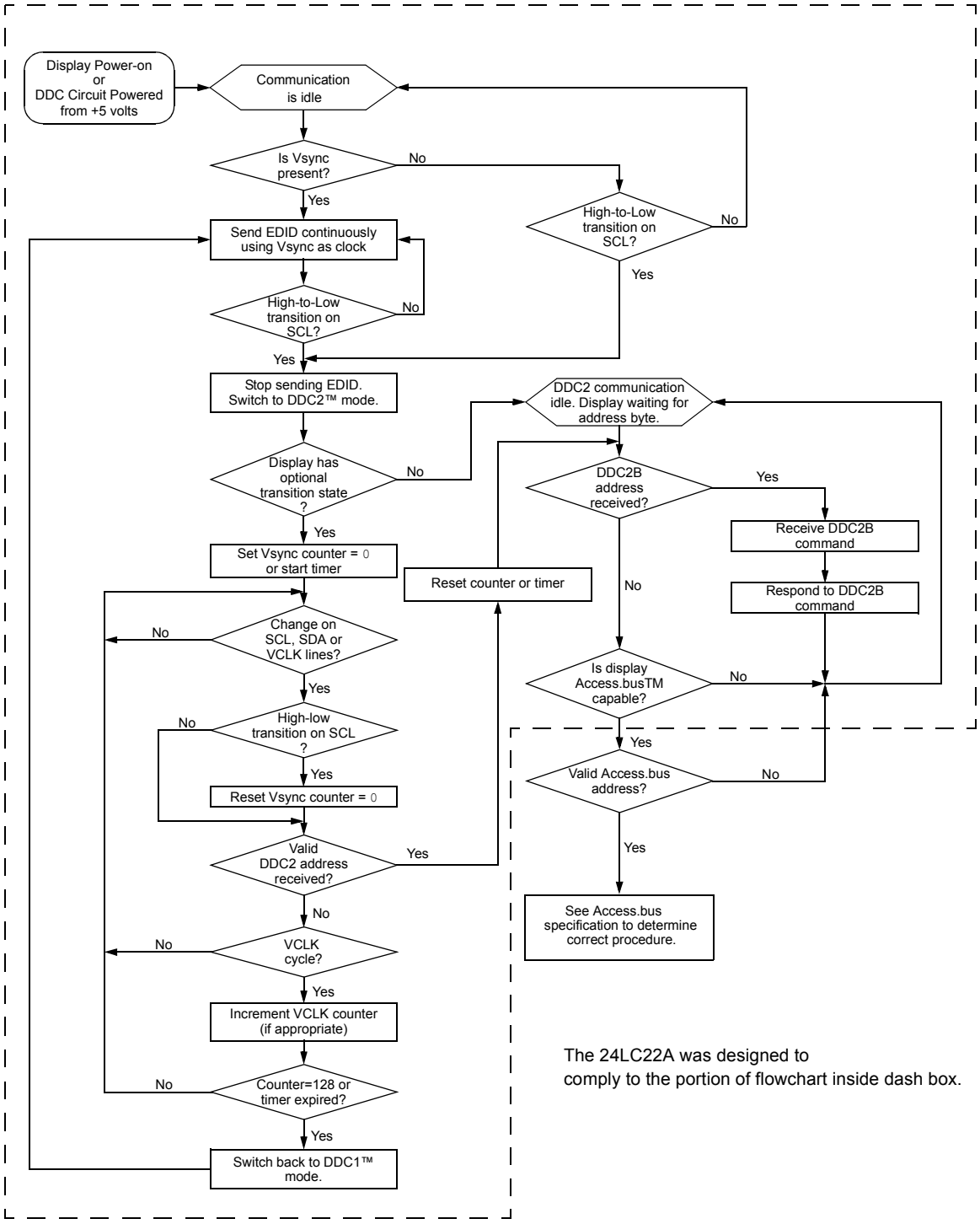


FIGURE 3-3: DISPLAY OPERATION PER DDC STANDARD PROPOSED BY VESA®



Note 1: The base flowchart is copyright © 1993, 1994, 1995 Video Electronic Standard Association (VESA) from VESA's Display Data Channel (DDC) Standard Proposal ver. 2p rev. 0, used by permission of VESA.

2: The dash box and text "The 24LC21A and... inside dash box." are added by Microchip Technology Inc.

3: Vsync signal is normally used to derive a signal for VCLK pin on the 24LCS22A.

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3.1 Bidirectional Mode Bus Characteristics

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 3-4).

3.1.1 BUS NOT BUSY (A)

Both data and clock lines remain high.

3.1.2 START DATA TRANSFER (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.1.3 STOP DATA TRANSFER (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

3.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur it will replace data in a first-in first-out (FIFO) fashion.

Note:	Once switched into Bidirectional mode, the 24LC22A will remain in that mode until power is removed. Removing power is the only way to reset the 24LC22A into the Transmit-Only mode.

3.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an Acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24LC22A does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition.

FIGURE 3-4: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

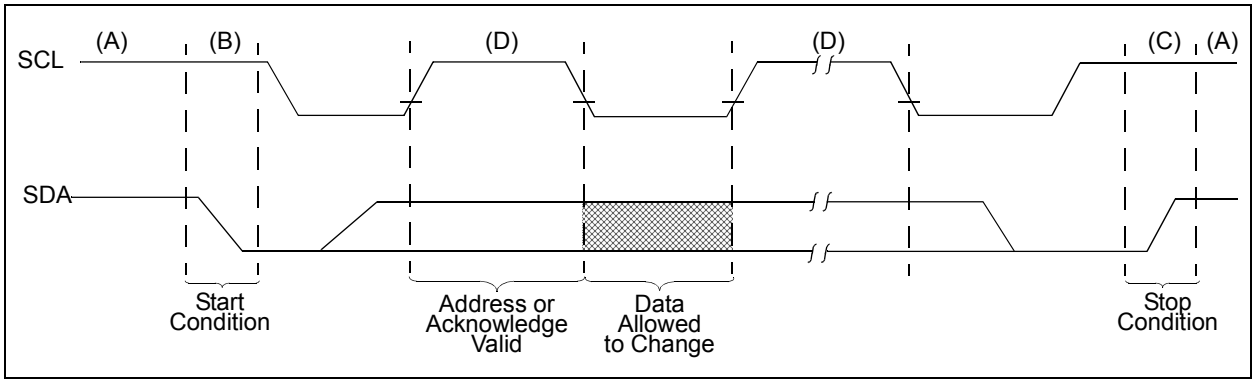


FIGURE 3-5: BUS TIMING START/STOP

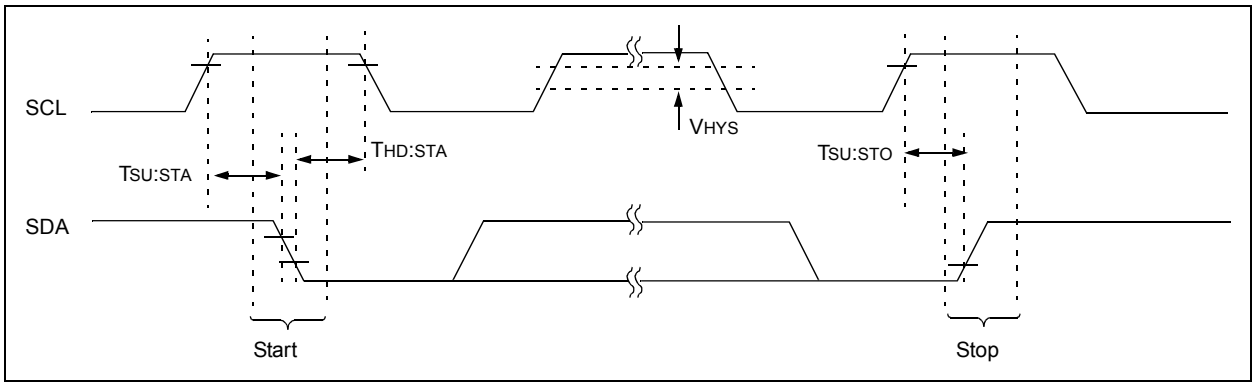
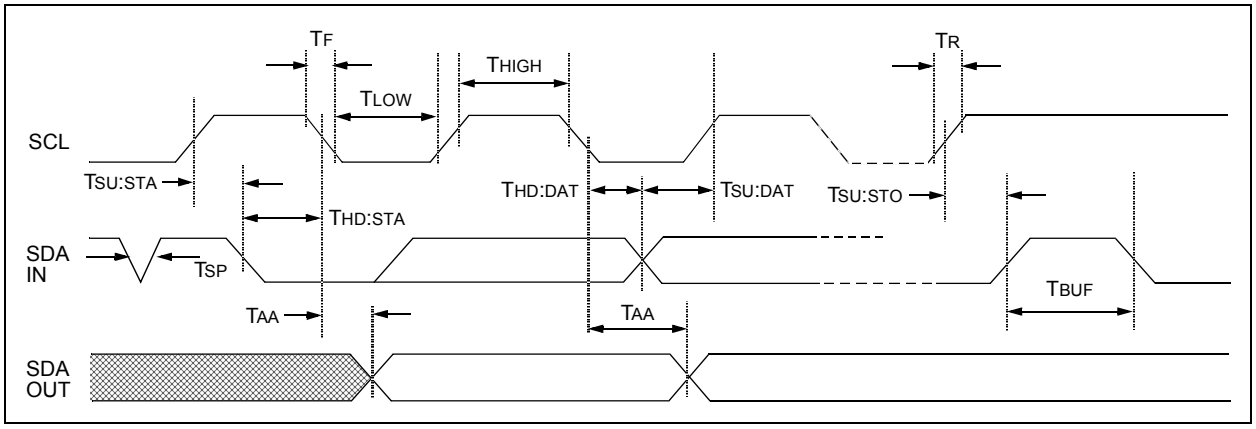


FIGURE 3-6: BUS TIMING DATA



3.1.6 SLAVE ADDRESS

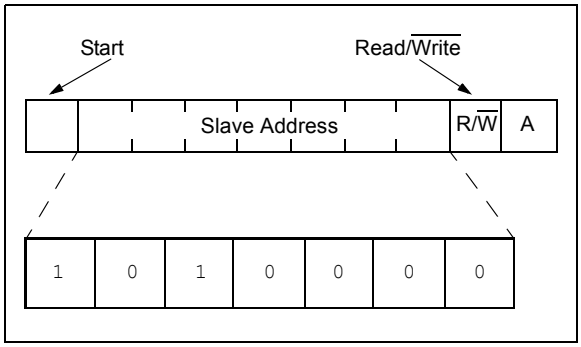
After generating a Start condition, the bus master transmits the slave address consisting of a 7-bit device code (1010000) for the 24LC22A.

The eighth bit of slave address determines whether the master device wants to read or write to the 24LC22A (Figure 3-7).

The 24LC22A monitors the bus for its corresponding slave address continuously. It generates an Acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Slave Address	R/$\overline{W}$
Read	1010000	1
Write	1010000	0

FIGURE 3-7: CONTROL BYTE ALLOCATION



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4.0 WRITE OPERATION

4.1 Byte Write

Following the Start signal from the master, the slave address (four bits), three zero bits (000) and the R/$\overline{W}$ bit which is a logic low are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the Address Pointer of the 24LC22A. After receiving another Acknowledge signal from the 24LC22A the master device will transmit the data word to be written into the addressed memory location. The 24LC22A acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and during this time the 24LC22A will not generate Acknowledge signals (Figure 4-1).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high-to-low during the self-timed program operation will not halt programming of the device.

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC22A in the same way as in a byte write. But instead of generating a Stop condition the master transmits up to eight data bytes to the 24LC22A, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a Stop condition. After the receipt of each word, the three lower order Address Pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received an internal write cycle will begin (Figure 4-3).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high-to-low during the self-timed program operation will not halt programming of the device.

Note:	Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 4-1: BYTE WRITE

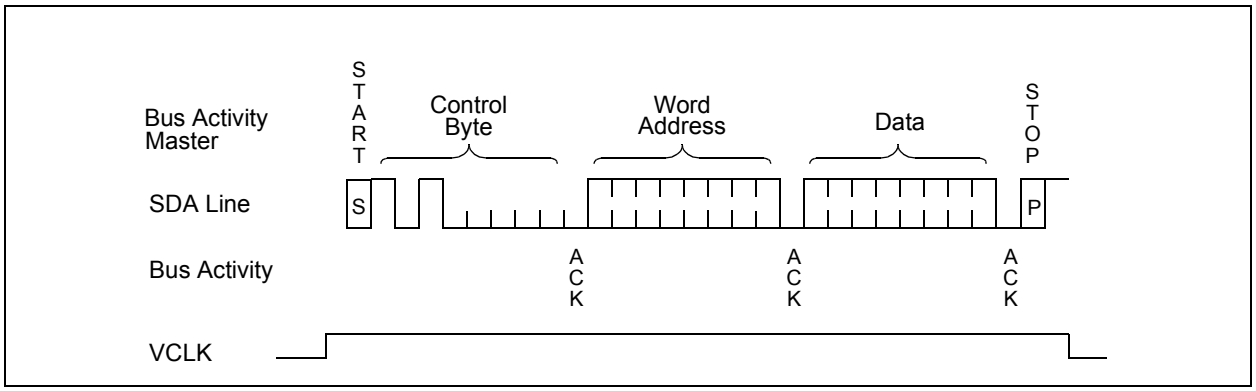


FIGURE 4-2: VCLK WRITE ENABLE TIMING

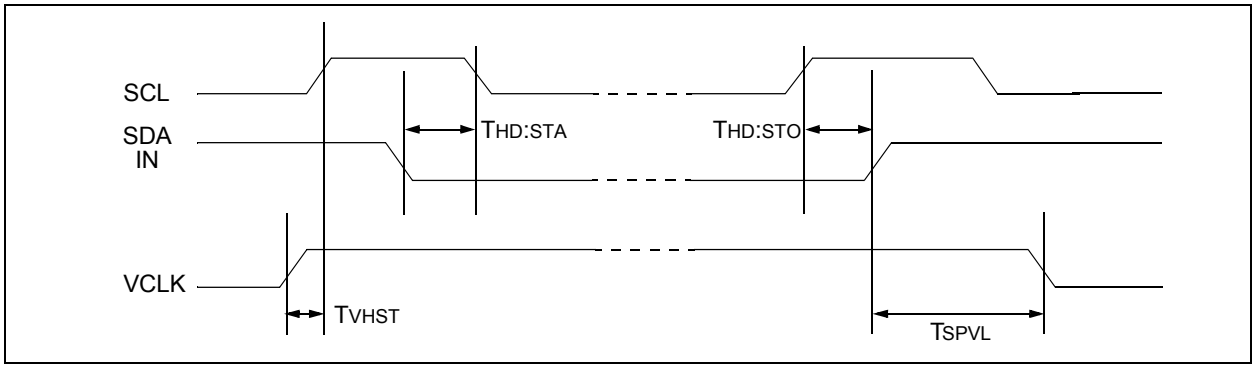
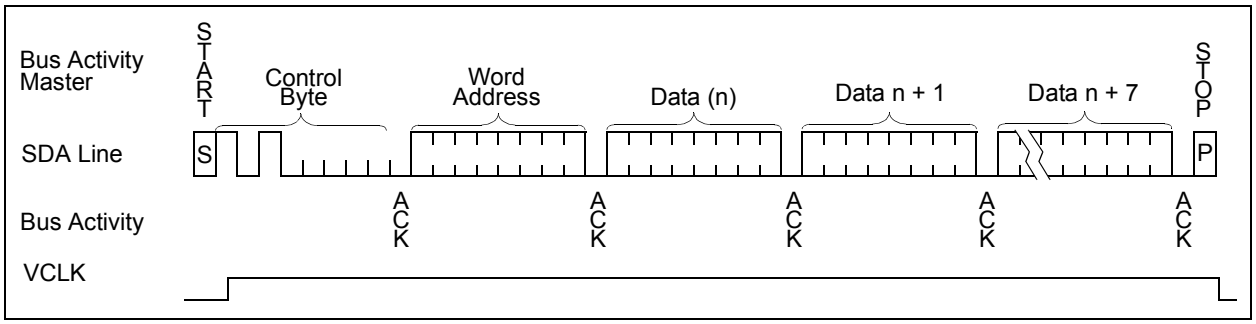


FIGURE 4-3: PAGE WRITE

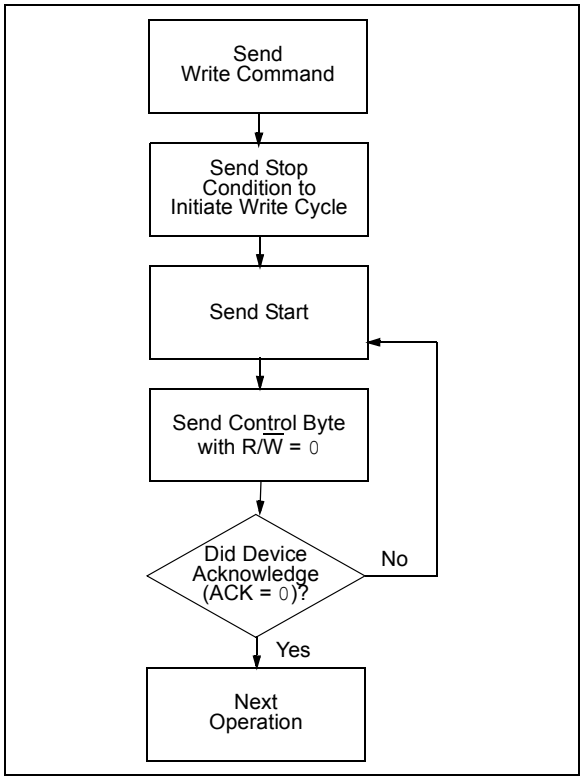


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5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

When using the 24LC22A in the Bidirectional mode, the VCLK pin can be used as a write-protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to VSS would allow the 24LC22A to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only mode.

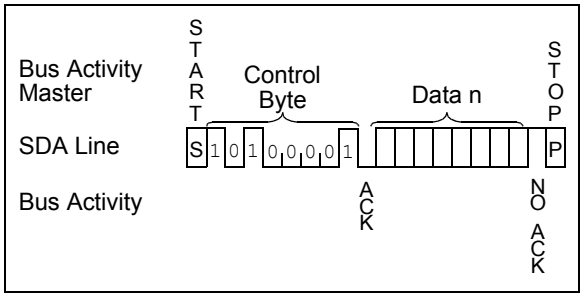
7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current Address Read

The 24LC22A contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC22A issues an acknowledge and transmits the eight-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24LC22A discontinues transmission (Figure 7-1).

FIGURE 7-1: CURRENT ADDRESS READ



7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC22A as part of a write operation. After the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC22A will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24LC22A discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC22A transmits the first data byte, the master issues an acknowledge as opposed to a Stop condition in a random read. This directs the 24LC22A to transmit the next sequentially addressed 8-bit word (Figure 7-3).

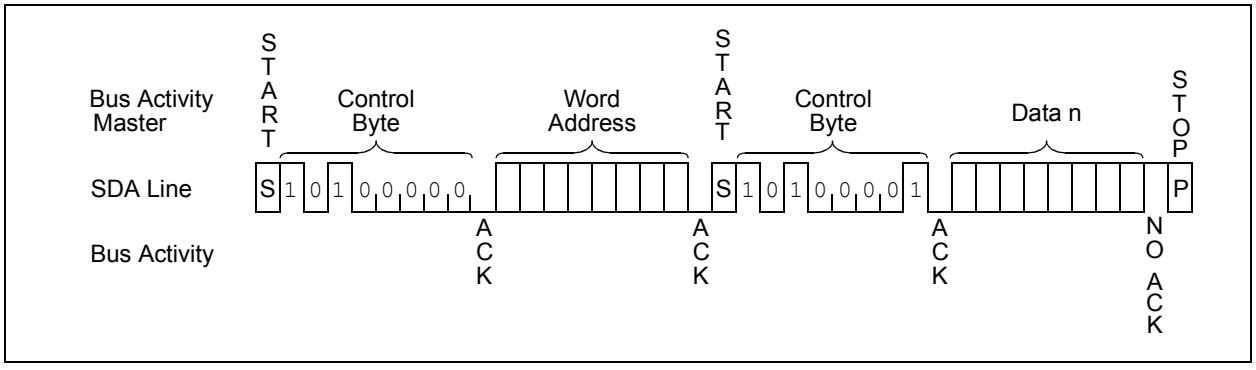
To provide sequential reads the 24LC22A contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC22A employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.5 volts at nominal conditions.

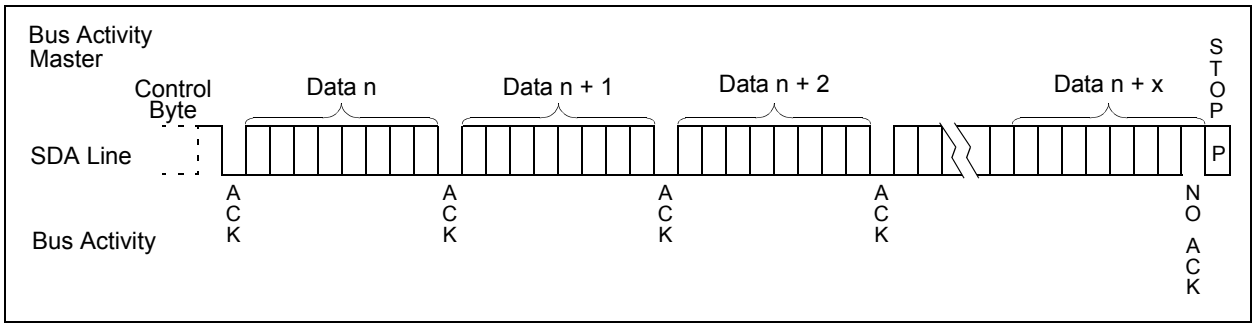
The SDA, SCL and VCLK inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-2: RANDOM READ



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FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 8-1.

TABLE 8-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock (Bidirectional mode)
VCLK	Serial Clock (Transmit-Only mode)
VCC	+2.5V to 5.5V Power Supply
NC	No Internal Connection

8.1 Serial Address/Data Input/Output (SDA)

This pin is used to transfer addresses and data into and out of the device, when the device is in the Bidirectional mode. In the Transmit-Only mode, which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open drain terminal, therefore the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer in the Bidirectional mode, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

8.2 Serial Clock (SCL)

This pin is the clock input for the Bidirectional mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit-Only mode to the Bidirectional mode. It must remain high for the chip to continue operation in the Transmit-Only mode.

8.3 Serial Clock (VCLK)

This pin is the clock input for the Transmit-Only mode (DDC1). In the Transmit-Only mode, each bit is clocked out on the rising edge of this signal. In the Bidirectional mode, a high logic level is required on this pin to enable write capability.

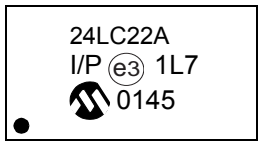
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

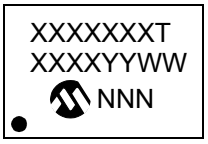
8-Lead PDIP (300 mil)



Example



8-Lead SOIC (3.90 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

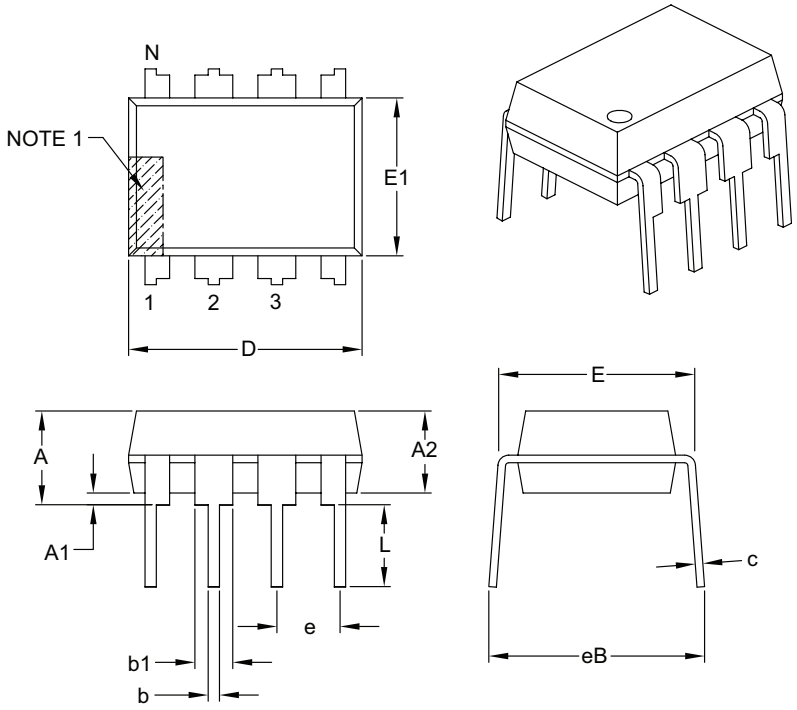
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code).

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8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

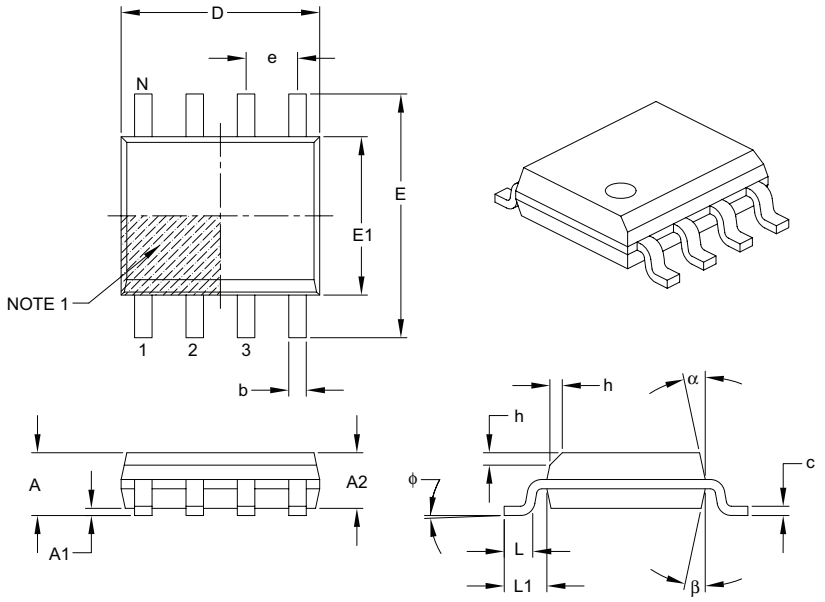
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

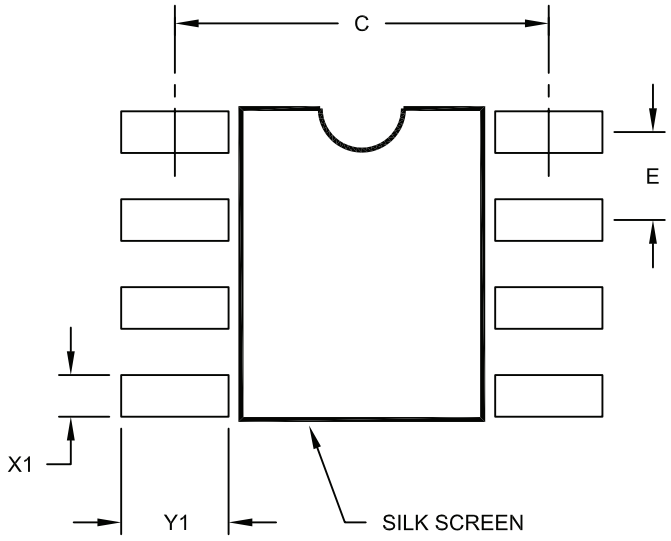
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

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8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

APPENDIX A: REVISION HISTORY

Revision A

Original release of document.

Revision B (10/2007)

Revised Features (added Pb-free); Revised ambient temperature; Revised Table 1.1, Para. D8 and D9; Revised Packaging Information; Replaced Package Drawings; Replaced On-Line Support; Revised Product ID System.

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PART NO.	X	/XX
Device	Temperature Range	Package

Device:	24LC22A:	2K VESA E-EDID Serial EEPROM
	24LC22AT:	2K VESA E-EDID Serial EEPROM (Tape and Reel)
Temperature Range:	I =	-40°C to +85°C
Package:	P =	Plastic DIP (300 mil Body), 8-Lead
	SN =	Plastic SOIC (3.90 mm Body), 8-Lead

Examples:

a) 24LC22A-I/P: Industrial temperature, PDIP package.

b) 24LC22A-I/SN: Industrial temperature, SOIC package.

c) 24LC22AT-I/SN: Tape and Reel, Industrial temperature, SOIC package.

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