24LC21A

1K 2.5V Dual Mode I²C™ Serial EEPROM

Features

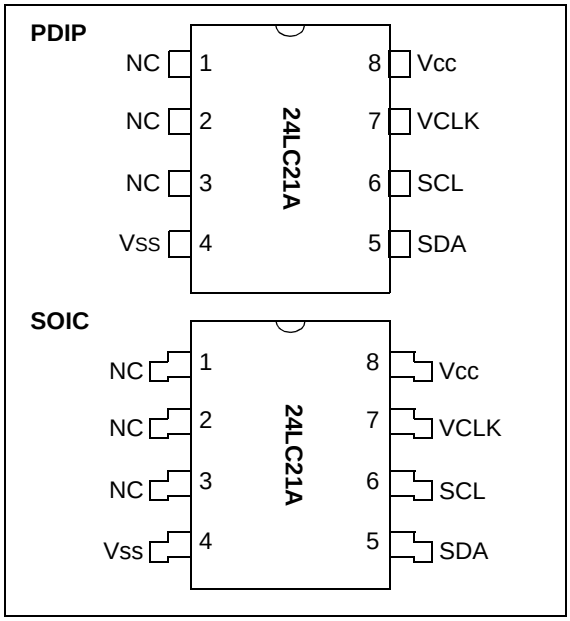
- Single supply with operation down to 2.5V
- Completely implements DDC1™/DDC2™ interface for monitor identification, including recovery to DDC1
- Pin and function compatible with 24LC21
- Low-power CMOS technology
  - 1 mA typical active current
  - 10 µA standby current typical at 5.5V
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page write buffer for up to eight bytes
- 1,000,000 erase/write cycles ensured
- Data retention > 200 years
- ESD Protection > 4000V
- 8-pin PDIP and SOIC package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

Description

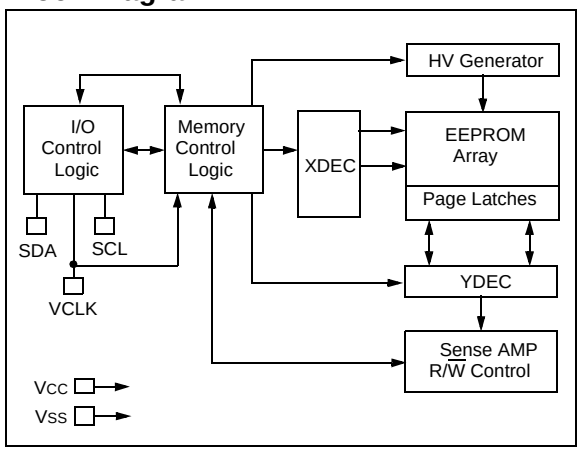
The Microchip Technology Inc. 24LC21A is a 128 x 8-bit dual-mode Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: Transmit-only mode and Bidirectional mode. Upon power-up, the device will be in the Transmit-only mode, sending a serial bit stream of the memory array from 00h to 7Fh, clocked by the VCLK pin. A valid high-to-low transition on the SCL pin will cause the device to enter the transition mode, and look for a valid control byte on the I²C bus. If it detects a valid control byte from the master, it will switch into Bidirectional mode, with byte selectable read/write capability of the memory array using SCL. If no control byte is received, the device will revert to the Transmit-only mode after it receives 128 consecutive VCLK pulses while the SCL pin is idle. The 24LC21A is available in a standard 8-pin PDIP and SOIC package in both commercial and industrial temperature ranges.

DDC is a trademark of the Video Electronics Standards Association.
I²C is a trademark of Philips Corporation.

Package Types



Block Diagram



Pin Function Table

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock (Bidirectional mode)
VCLK	Serial Clock (Transmit-only mode)
Vcc	+2.5V to 5.5V Power Supply
NC	No Connection

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

V_{CC}.....7.0V

All inputs and outputs w.r.t. V_{SS}.....-0.6V to V_{CC} +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-65°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS	V_{CC} = +2.5V to 5.5V Commercial (C): T_A = 0°C to +70°C Industrial (I): T_A =-40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
SCL and SDA pins:					
High-level input voltage	V_{IH}	0.7 V_{CC}	—	V	
Low-level input voltage	V_{IL}	—	0.3 V_{CC}	V	
Input levels on VCLK pin:					
High-level input voltage	V_{IH}	2.0	—	V	V_{CC} ≥ 2.7V **(Note)**
Low-level input voltage	V_{IL}	—	0.2 V_{CC}	V	V_{CC} < 2.7V **(Note)**
Hysteresis of Schmitt Trigger inputs	V_{HYS}	.05 V_{CC}	—	V	**(Note)**
Low-level output voltage	V_{OL1}	—	0.4	V	I_{OL} = 3 mA, V_{CC} = 2.5V **(Note)**
Low-level output voltage	V_{OL2}	—	0.6	V	I_{OL} = 6 mA, V_{CC} = 2.5V
Input leakage current	I_{LI}	—	±1	µA	V_{IN} = 0.1V to V_{CC}
Output leakage current	I_{LO}	—	±1	µA	V_{OUT} = 0.1V to V_{CC}
Pin capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	10	pF	V_{CC} = 5.0V **(Note)** T_A = 25°C, F_{CLK} = 1 MHz
Operating current	I_{CC} Write	—	3	mA	V_{CC} = 5.5V
	I_{CC} Read	—	1	mA	V_{CC} = 5.5V, SCL = 400 kHz
Standby current	I_{CCS}	—	30	µA	V_{CC} = 3.0V, SDA = SCL = V_{CC}
		—	100	µA	V_{CC} = 5.5V, SDA = SCL = V_{CC} V_{CLK} = V_{SS}

Note: This parameter is periodically sampled and not 100% tested.

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TABLE 1-2: AC CHARACTERISTICS

Parameter	Symbol	Vcc= 2.5-5.5V Standard Mode		Vcc= 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	**(Note 1)**
SDA and SCL fall time	TF	—	300	—	300	ns	**(Note 1)**
Start condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
Start condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated Start condition
Data input hold time	THD:DAT	0	—	0	—	ns	**(Note 2)**
Data input setup time	TSU:DAT	250	—	100	—	ns	
Stop condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	**(Note 2)**
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 + 0.1 CB	250	ns	**(Note 1)**, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	**(Note 3)**
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
VCLK setup time	TVHST	0	—	0	—	ns	
VCLK hold time	TSPVL	4000	—	600	—	ns	
Mode transition time	TVHZ	—	1000	—	500	ns	
Transmit-only power-up time	TVPU	0	—	0	—	ns	
Input filter spike suppression (VCLK pin)	TSPV	—	100	—	100	ns	
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block mode **(Note 4)**

Note 1: Not 100% tested. CB = Total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to Schmitt Trigger inputs which provide noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our web site.

2.0 FUNCTIONAL DESCRIPTION

The 24LC21A is designed to comply to the DDC Standard proposed by VESA (Figure 3-3) with the exception that it is not Access.bus capable. It operates in two modes, the Transmit-only mode and the Bidirectional mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input but sharing a common data line (SDA). The device enters the Transmit-only mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high-to-low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the Bidirectional mode and look for its control byte to be sent by the master. If it detects its control byte, it will stay in the Bidirectional mode. Otherwise, it will revert to the Transmit-only mode after it sees 128 VCLK pulses.

2.1 Transmit-Only Mode

The device will power-up in the Transmit-only mode at address 00H. This mode supports a unidirectional 2-wire protocol for continuous transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-only mode (**Section 2.2 "Initialization Procedure"**). In this mode, data is transmitted on the SDA pin in 8-bit bytes, with each byte followed by a ninth, null bit (Figure 2-1). The clock source for the Transmit-only mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted Most Significant bit first. Each byte within the memory array will be output in sequence. After address 7Fh in the memory array is transmitted, the internal address pointers will wrap around to the first memory location (00h) and continue. The Bidirectional mode Clock (SCL) pin must be held high for the device to remain in the Transmit-only mode.

2.2 Initialization Procedure

After VCC has stabilized, the device will be in the Transmit-only mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal sychronization. During this period, the SDA pin will be in a high-impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the Most Significant bit in address 00h. (Figure 2-2).

FIGURE 2-1: TRANSMIT-ONLY MODE

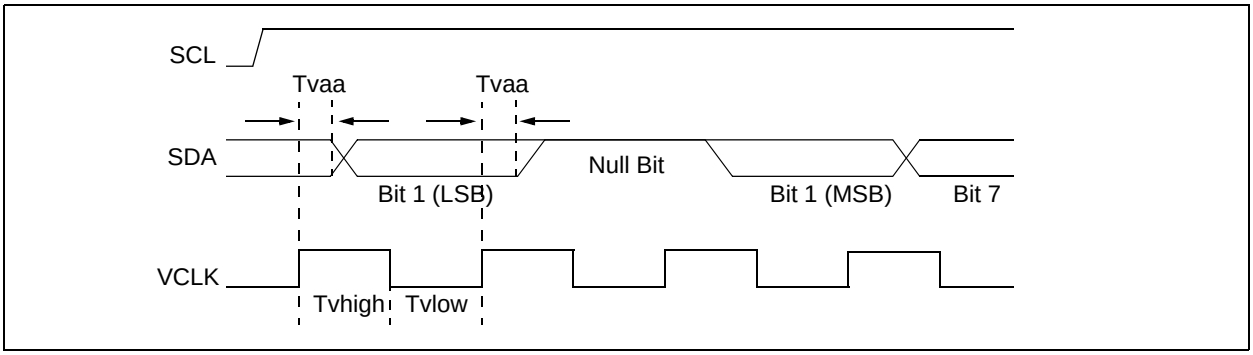
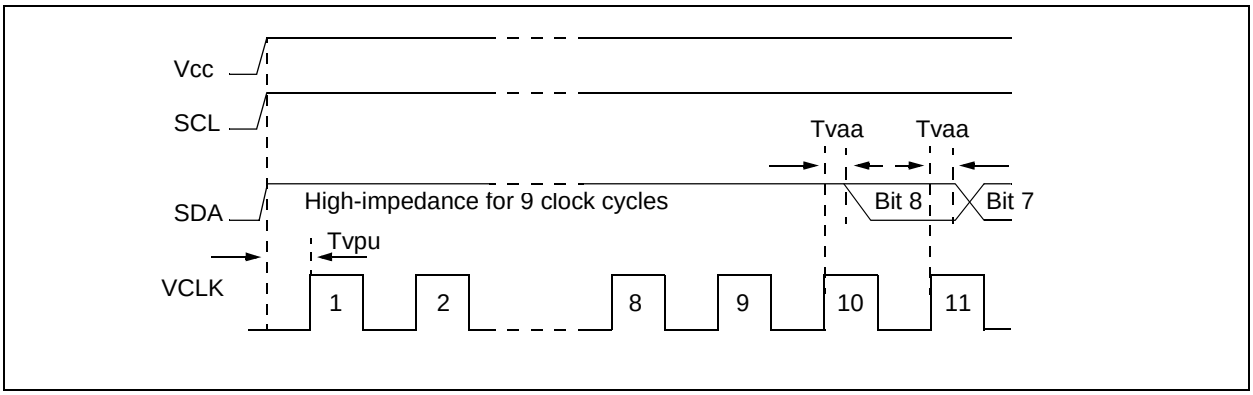


FIGURE 2-2: DEVICE INITIALIZATION



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3.0 BIDIRECTIONAL MODE

Before the 24LC21A can be switched into the Bidirectional mode (Figure 3-1), it must enter the Transition mode, which is done by applying a valid high-to-low transition on the Bidirectional mode Clock (SCL). As soon it enters the Transition mode, it looks for a control byte 1010 000X on the I^2C™ bus, and starts to count pulses on VCLK. Any high-to-low transition on the SCL line will reset the count. If it sees a pulse count of 128 on VCLK while the SCL line is idle, it will revert back to the Transmit-only mode, and transmit its contents starting with the Most Significant bit in address 00h. However, if it detects the control byte on the I^2C™ bus, (Figure 3-2) it will switch to the in the Bidirectional mode. Once the device has made the transition to the Bidirectional mode, the only way to switch the device back to the Transmit-only mode is to remove power from the device. The mode transition process is shown in detail in Figure 3-3.

Once the device has switched into the Bidirectional mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two-wire Bidirectional data transmission protocol (I^2C™). In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bidirectional mode Clock (SCL), controls access to the bus and generates the Start and Stop conditions, while the 24LC21A acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. In the Bidirectional mode, the 24LC21A only responds to commands for device 1010 000X.

FIGURE 3-1: MODE TRANSITION WITH RECOVERY TO TRANSMIT-ONLY MODE

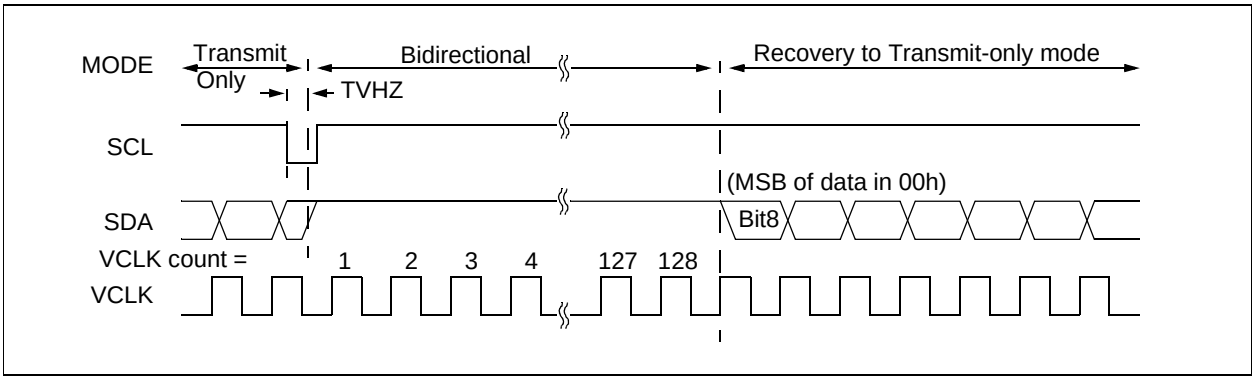


FIGURE 3-2: SUCCESSFUL MODE TRANSITION TO BIDIRECTIONAL MODE

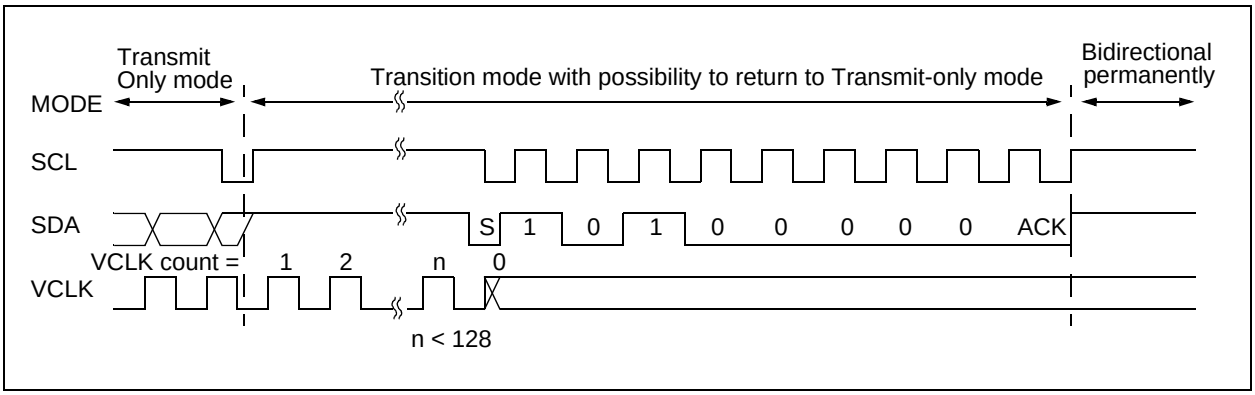
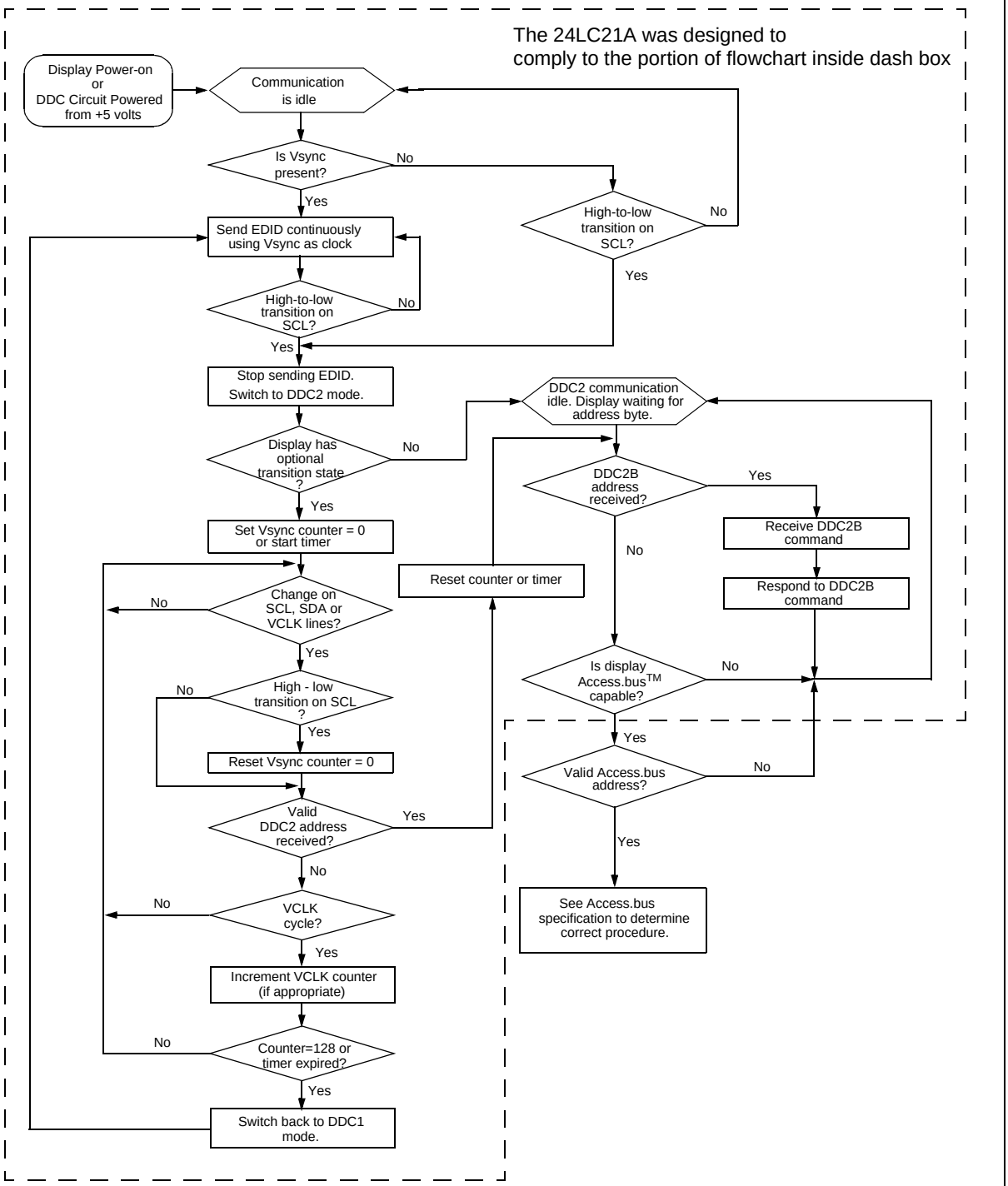


FIGURE 3-3: DISPLAY OPERATION PER DDC STANDARD PROPOSED BY VESA



Note 1: The base flowchart is copyright © 1993, 1994, 1995 Video Electronic Standard Association (VESA) from VESA's Display Data Channel (DDC) Standard Proposal ver. 2p rev. 0, used by permission of VESA.

2: The dash box and text "The 24LC21A and... inside dash box." are added by Microchip Technology Inc.

3: Vsync signal is normally used to derive a signal for VCLK pin on the 24LC21A.

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3.1 Bidirectional Mode Bus Characteristics

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 3-4).

3.1.1 BUS NOT BUSY (A)

Both data and clock lines remain high.

3.1.2 START DATA TRANSFER (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.1.3 STOP DATA TRANSFER (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

3.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

Note:	Once switched into Bidirectional mode, the 24LC21A will remain in that mode until power is removed. Removing power is the only way to reset the 24LC21A into the Transmit-only mode.

3.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24LC21A does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition.

FIGURE 3-4: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

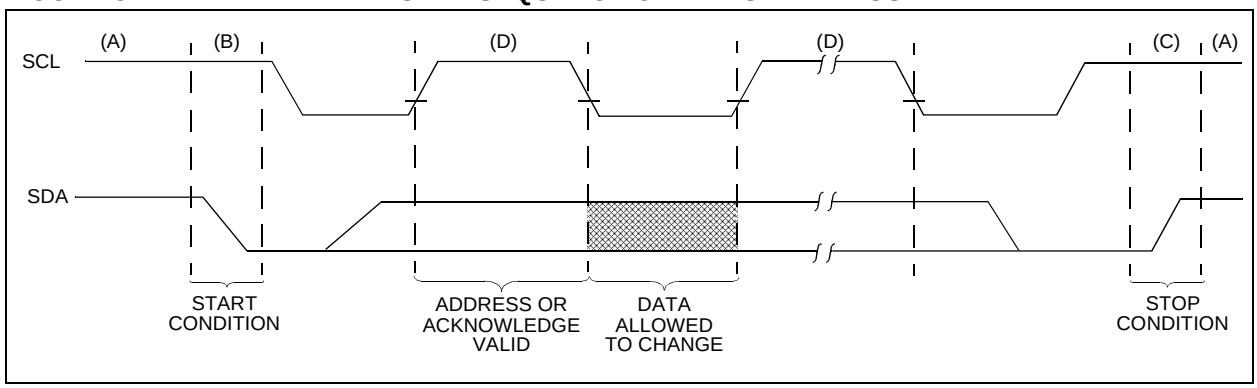


FIGURE 3-5: BUS TIMING START/STOP

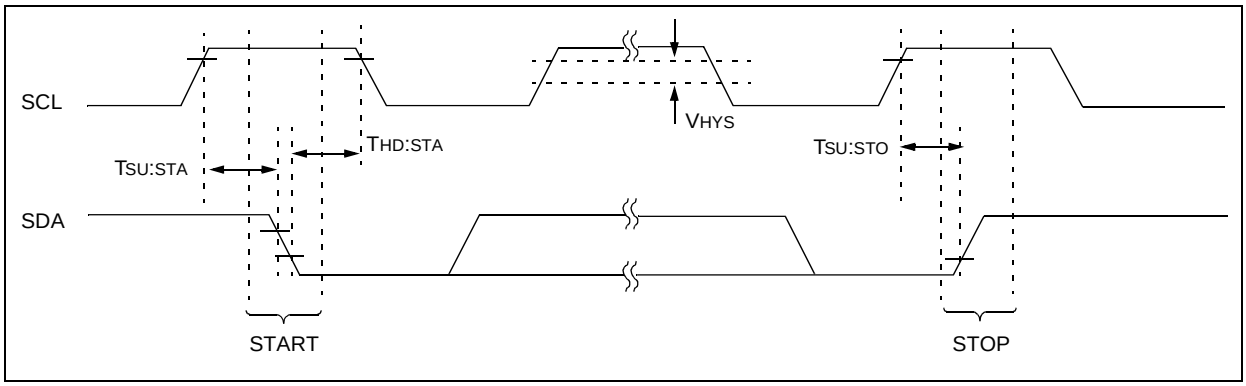
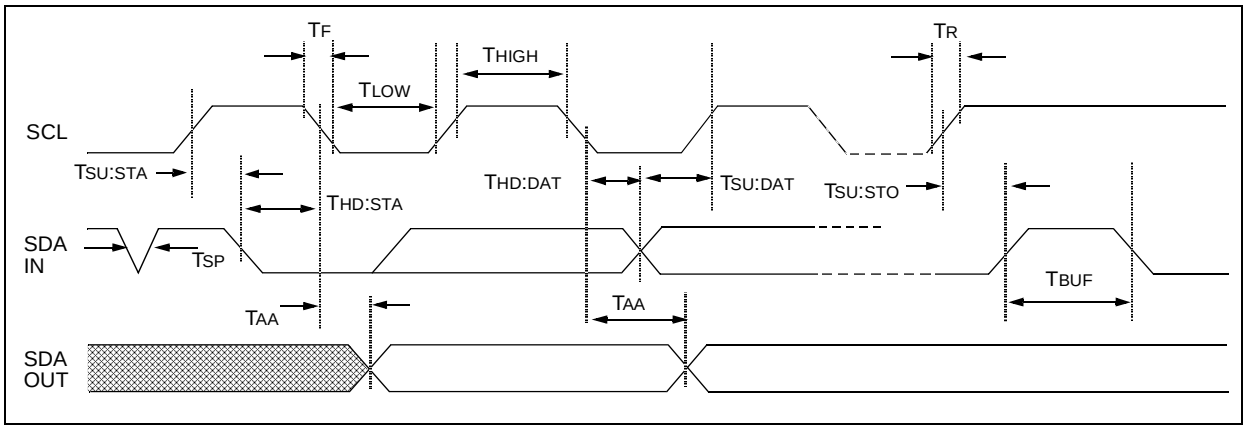


FIGURE 3-6: BUS TIMING DATA



3.1.6 SLAVE ADDRESS

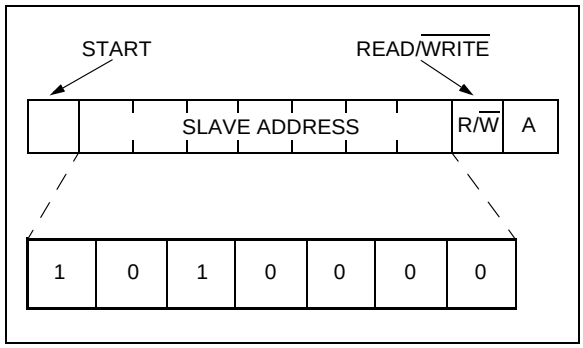
After generating a Start condition, the bus master transmits the slave address consisting of a 7-bit device code (1010000) for the 24LC21A.

The eighth bit of slave address determines whether the master device wants to read or write to the 24LC21A (Figure 3-7).

The 24LC21A monitors the bus for its corresponding slave address continuously. It generates an Acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Slave Address	R/$\overline{W}$
Read	1010000	1
Write	1010000	0

FIGURE 3-7: CONTROL BYTE ALLOCATION



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4.0 WRITE OPERATION

4.1 Byte Write

Following the start signal from the master, the slave address (four bits), three zero bits (000) and the R/$\overline{W}$ bit which is a logic low are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC21A. After receiving another acknowledge signal from the 24LC21A the master device will transmit the data word to be written into the addressed memory location. The 24LC21A acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and during this time the 24LC21A will not generate acknowledge signals (Figure 4-1).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high-to-low during the self-timed program operation will not halt programming of the device.

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC21A in the same way as in a byte write. But instead of generating a Stop condition the master transmits up to eight data bytes to the 24LC21A which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a Stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received an internal write cycle will begin (Figure 4-3).

It is required that VCLK be held at a logic high level during command and data transfer in order to program the device. This applies to both byte write and page write operation. Note, however, that the VCLK is ignored during the self-timed program operation. Changing VCLK from high-to-low during the self-timed program operation will not halt programming of the device.

Note:	Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 4-1: BYTE WRITE

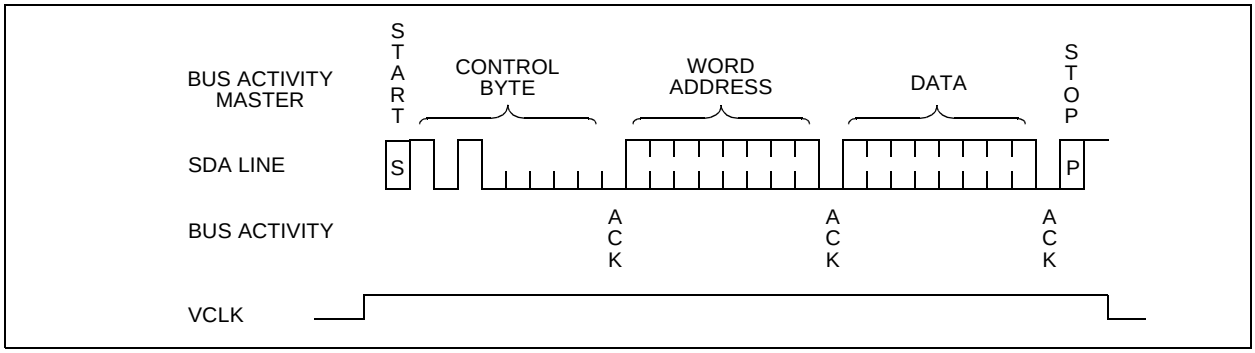


FIGURE 4-2: VCLK WRITE ENABLE TIMING

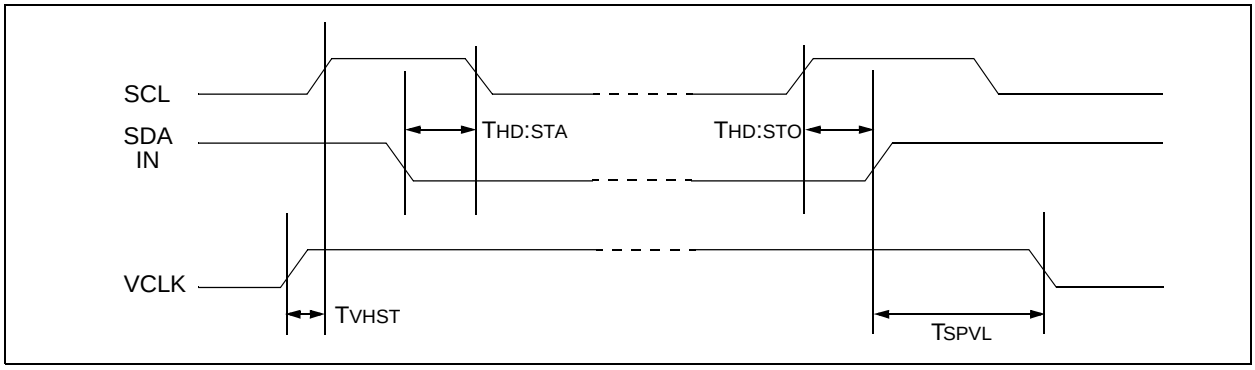
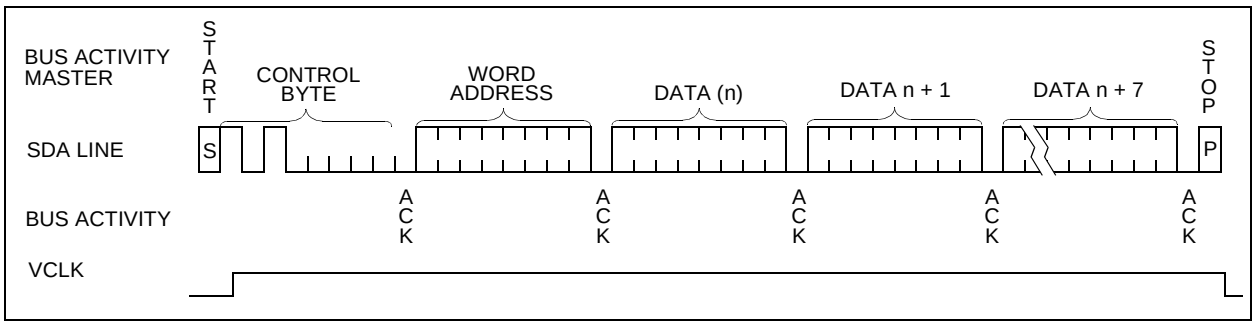


FIGURE 4-3: PAGE WRITE

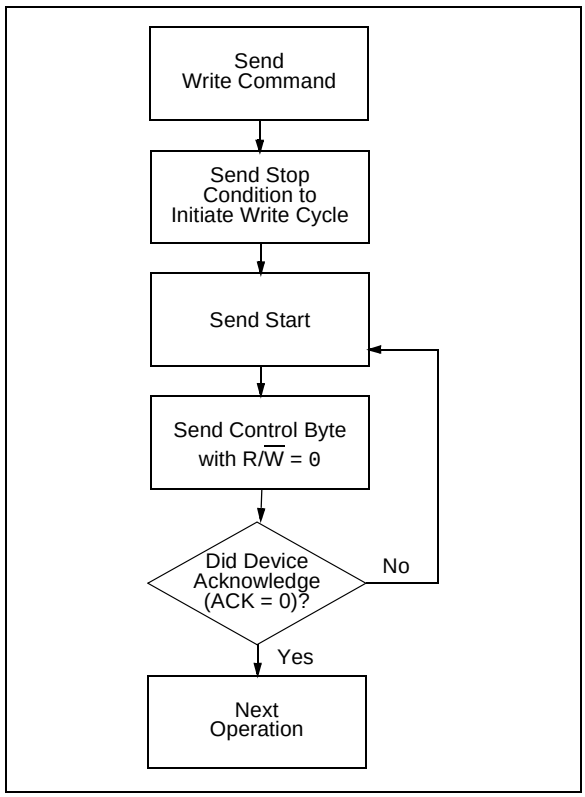


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5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

When using the 24LC21A in the Bidirectional mode, the VCLK pin can be used as a write-protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to VSS would allow the 24LC21A to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-only mode.

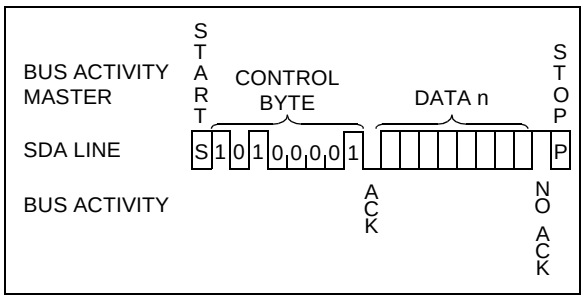
7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current Address Read

The 24LC21A contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC21A issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24LC21A discontinues transmission (Figure 7-1).

FIGURE 7-1: CURRENT ADDRESS READ



7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC21A as part of a write operation. After the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC21A will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24LC21A discontinues transmission (Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC21A transmits the first data byte, the master issues an acknowledge as opposed to a Stop condition in a random read. This directs the 24LC21A to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24LC21A contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC21A employs a V_{CC} threshold detector circuit which disables the internal erase/write logic if the V_{CC} is below 1.5 volts at nominal conditions.

The SDA, SCL and VCLK inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

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FIGURE 7-2: RANDOM READ

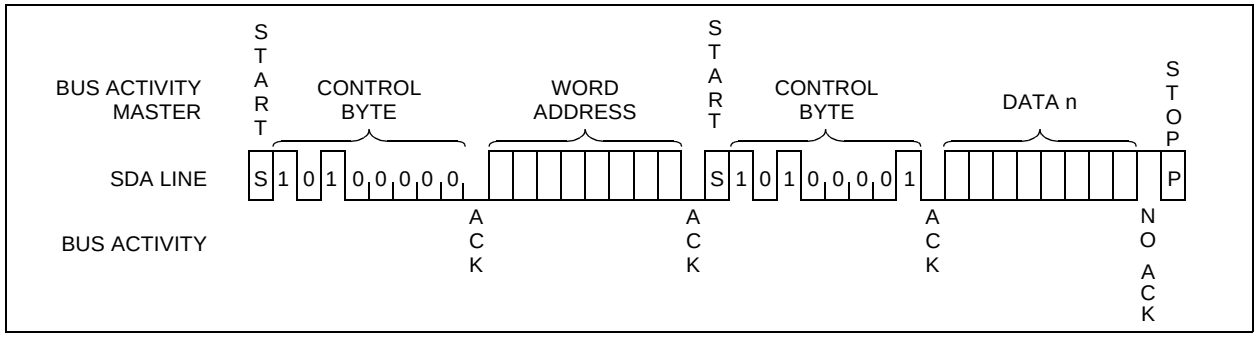
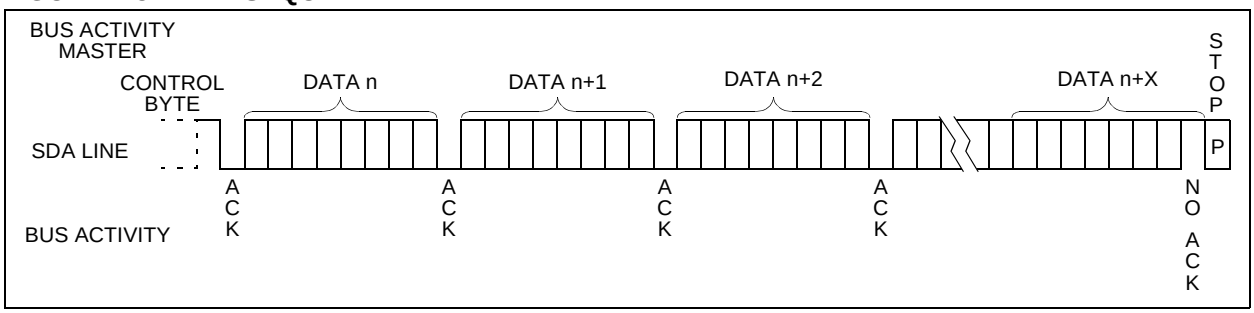


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the Bidirectional mode. In the Transmit-only mode, which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open drain terminal, therefore the SDA bus requires a pull-up resistor to VCC (typical 10 KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer in the Bidirectional mode, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

8.2 SCL

This pin is the clock input for the Bidirectional mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit-only mode to the Bidirectional mode. It must remain high for the chip to continue operation in the Transmit-only mode.

8.3 VCLK

This pin is the clock input for the Transmit-only mode (DDC1). In the Transmit-only mode, each bit is clocked out on the rising edge of this signal. In the Bidirectional mode, a high logic level is required on this pin to enable write capability.

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APPENDIX A: REVISION HISTORY

Revision F

Corrections to Section 1.0, Electrical Characteristics.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	24LC21A	Dual Mode Serial EEPROM
	24LC21AT	Dual Mode Serial EEPROM (Tape and Reel)
Temperature Range	Blank	0°C to +70°C
	I	-40°C to +85°C
Package	P =	Plastic DIP (300 mil Body), 8-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead

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