64KI²C™ CMOS Serial EFPROM

DEVICE SELECTION TABLE

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
24AA64	1.8-5.5V	400 kHz †	I
24LC64	2.5-5.5V	400 kHz‡	I,E

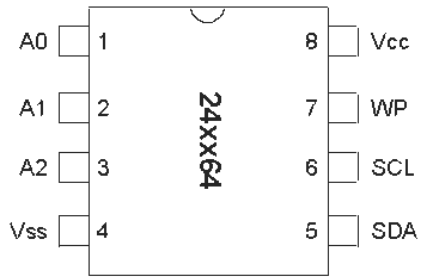
†100kHz for V_{CC}<2.5V.
‡100kHz for E temperature range.

FEATURES

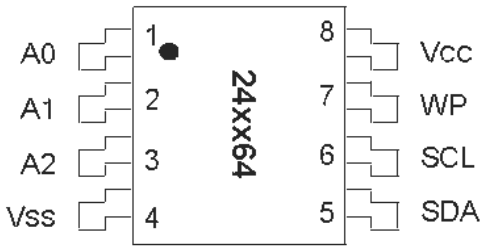
- Low power CMOS technology
  - -Maximum write current 3 mA at 5.5V
  - -Maximum read current 400μA at 5.5V
  - -Standby current 100nA typical at 5.5V
- 2-wire serial interface bus, I²C compatible
- Cascadable for up to eight devices
- Self-timed ERASE/WRITE cycle
- 32-byte page or byte write modes available
- 5 ms max write cycle time
- Hardware write protect for entire array
- Output slope control to eliminate ground bounce
- Schmitt trigger inputs for noise suppression
- 1,000,000 erase/write cycles guaranteed
- Electrostatic discharge protection>4000V
- Data retention >200 years
- 8-pin PDIP, SDIC (150 and 208 mil) and TSSOP packages; 14-pin SOIC package
- Temperature ranges:
  - -Industrial (I): -40°C to +85°C
  - -Automotive (E) -40°C to +125°C

PACKAGE TYPE

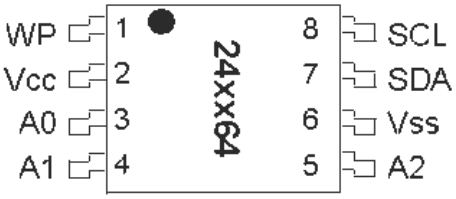
PDIP



SOIC



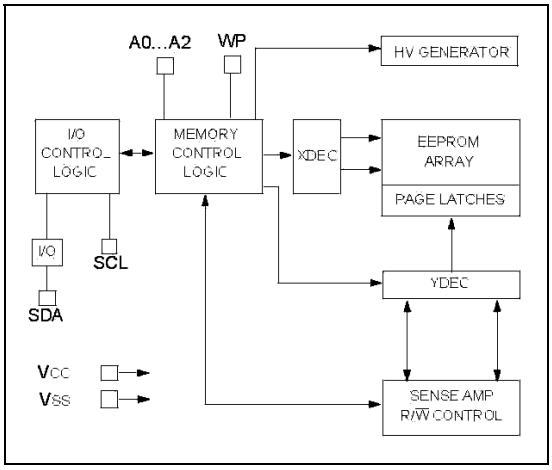
TSSOP



DESCRIPTION

The Artschip Technology Inc. 24AA64/24LC64 (24xx64*) is a 8K x8 (64k bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (1.8 V to 5.5V). It has been developed for advanced, low power applications such as personal communications or data acquisition. This device also has a page-write capability of up to 32 bytes of data. This device is capable of both random and sequential reads up to the 64K boundary. Functional address lines allow up to eight devices on the same bus, for up to 512 kbits address space. This device is available in the standard 8-pin plastic DIP, 8-pin SOIC (150 and 208 mil), and 8-pin TSSOP.

BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc……..7.0V
All inputs and outputs w.r.t. Vss……-0.6V to Vcc +1.0V
Storage temperature……..-65°C to +150°C
Ambient temp. with power applied…….. -65°C to +125°C
Soldering temperature of leads (10 seconds)……+300°C
ESD protection on all pins…….. ≥4kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1 PIN FUNCTION TABLE

Name	Function
A0,A1,A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect Input
Vcc	+1.8 to 5.5V (24AA64) +2.5 to 5.5V (24LC64)

TABLE 1-2 DC CHARACTERISTICS

All parameters apply across the recommended operating ranges unless otherwise noted.	Industrial (I): Vcc=+1.8V to 5.5V Tamb =-40°C to +85°C Automotive (E): Vcc= 4.5 V to 5.5V Tamb =-40°C to 125°C				
Parameter	Symbol	Min	Max	Units	Conditions
A0,A1,A2, SCL, SDA, and WP pins:					
High level input voltage	V_{IH}	0.7 Vcc	—	V	
Low level input voltage	V_{IL}	—	0.3 Vcc	V	Vcc≥2.5V
			0.2Vcc	V	Vcc<2.5V
Hysteresis of Schmitt Trigger Inputs (SDA,SCL pins)	V_{HYS}	0.05 Vcc	—	V	Vcc>2.5V(Note)
Low level output voltage	V_{OL}	—	0.40	V	I_{OL} = 3.0 mA @ Vcc =4.5V I_{OL} = 2.1 mA @ Vcc =2.5V
Input leakage current	I_{LI}	-10	10	µA	V_{IN}=V_{SS} to Vcc, WP= Vss V_{IN}=Vss or Vcc, WP =Vcc
Output leakage current	I_{LO}	-10	10	µA	V_{OUT}=Vss to Vcc
Pin capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	10	pF	Vcc= 5.0V (Note) Tamb=25°C, f_C=1MHz
Operating current	Icc Write	—	3	mA	Vcc=5.5V
	Icc Read	—	400	µA	Vcc=5.5V, SCL =400KHz
Standby current	Iccs	—	1	µA	SCL=SDA=Vcc=5.5V A0,A1,A2,WP=Vss

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING DATA

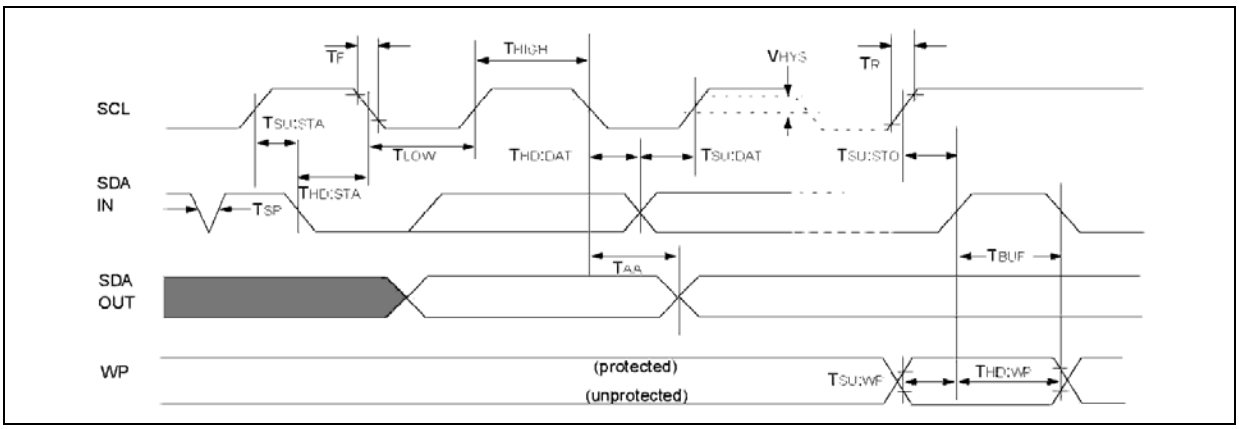


TABLE 1-3 AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Industrial (I): Vcc = +1.8V to 5.5V Tamb= -40°C to + 85°C Automotive (E): Vcc= +4.5V to 5.5V Tamb = -40°C to 125°C				
Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	F_{CLK}	— — —	100 100 400	kHz	4.5V≤Vcc ≤5.5V (E Temp range) 1.8V≤ Vcc ≤2.5V 2.5V≤Vcc≤5.5V
Clock high time	T_{HIGH}	4000 4000 600	— — —	ns	4.5V≤Vcc≤5.5V (E Temp range) 1.8V≤Vcc≤2.5V 2.5V≤Vcc≤5.5V
Clock low time	T_{LOW}	4700 4700 1300	— — —	ns	4.5V≤Vcc≤5.5V (E Temp range) 1.8V≤Vcc≤2.5V 2.5V≤Vcc≤5.5V
SDA and SCL rise time (Note 1)	T_R	— — —	1000 1000 300	ns	4.5V≤Vcc≤5.5V (E Temp range) 1.8V≤Vcc≤2.5V 2.5V≤Vcc≤5.5V
SDA and SCL fall time	T_F	—	300	ns	(Note 1)
START condition hold time	$T_{HD:STA}$	4000 4000 600	— — —	ns	4.5V≤Vcc≤5.5V (E Temp range) 1.8V≤Vcc≤2.5V 2.5V≤Vcc≤5.5V
START condition setup time	$T_{SU:STA}$	4700 4700 600	— — —	ns	4.5V≤Vcc≤5.5V (E Temp range) 1.8V≤Vcc≤2.5V 2.5V≤Vcc≤5.5V
Data input hold time	$T_{HD:DAT}$	0	—	ns	(Note 2)
Data input setup time	$T_{SU:DAT}$	250 250 100	— — —	ns	4.5V≤Vcc≤5.5V (E Temp range) 1.8V≤Vcc≤2.5V 2.5V≤Vcc≤5.5V
STOP condition setup time	$T_{SU:STO}$	4000 4000 600	— — —	ns	4.5V≤Vcc≤5.5V (E Temp range) 1.8V≤Vcc≤2.5V 2.5V≤Vcc≤5.5V
WP Setup time	$T_{SU:WP}$	4000 4000 600	— — —	ns	4.5V≤Vcc≤5.5V (E Temp range) 1.8V≤Vcc≤2.5V 2.5V≤Vcc≤5.5V
WP hold time	$T_{HD:WP}$	4700 4000 1300	— — —	ns	4.5V≤Vcc≤5.5V (E Temp range) 1.8V≤Vcc≤2.5V 2.5V≤Vcc≤5.5V
Output valid from clock (Note 2)	T_{AA}	— — —	3500 3500 900	ns	4.5V≤Vcc≤5.5V (E Temp range) 1.8V≤Vcc≤2.5V 2.5V≤Vcc≤5.5V
Bus free time: Time the bus must be free before a new transmission can start	T_{BUF}	4700 4700 1300	— — —	ns	4.5V≤Vcc≤5.5V (E Temp range) 1.8V≤Vcc≤2.5V 2.5V≤Vcc≤5.5V
Output fall time from V_{IH} Minimum to V_{IL} maximum	T_{OF}	10	250	ns	C_B ≤ 100pF (Note 1)
Input filter spike suppression (SDA and SCL pins)	T_{SP}	—	50	ns	(Notes 1 and 3)
Write cycle time (byte or page)	T_{WC}	—	5	ms	
Endurance		1M	—	cycles	25°C, Vcc=5.0V, Block Mode (Note 4)

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined Tsp and V_{HYS} specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specifications for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on Artschip's website.

2.0 PIN DESCRIPTIONS

2.1 A0,A1,A2 Chip Address Inputs

The A0,A1,A2 inputs are used by the 24xx64 for multiple device operation. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight devices may be connected to the same bus by using different chip select bit combinations. These inputs must be connected to either Vcc or Vss.

2.2 SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull up resistor to Vcc (typical 10kΩ for 100kHz, 2kΩ for 400kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.4 WP

This pin can be connected to either Vss, Vcc or left floating. An internal pull-down resistor on this pin will keep the device in the unprotected state if left floating. If tied to Vss or left floating, normal memory operation is enabled (read/write the entire memory 0000-1FFF).

If tied to Vcc, WRITE operations are inhibited. Read operations are not affected.

3.0 FUNCTIONAL DESCRIPTION

The 24xx64 supports a bi-directional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and stop conditions while the 24xx64 works as a slave. Both master and slave can operate as a transmitter or receiver but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly. The following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

4.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

4.3 Stop Data Transfer (C)

A Low to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must end with a STOP condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

> Note: The 24xx64 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24xx64) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

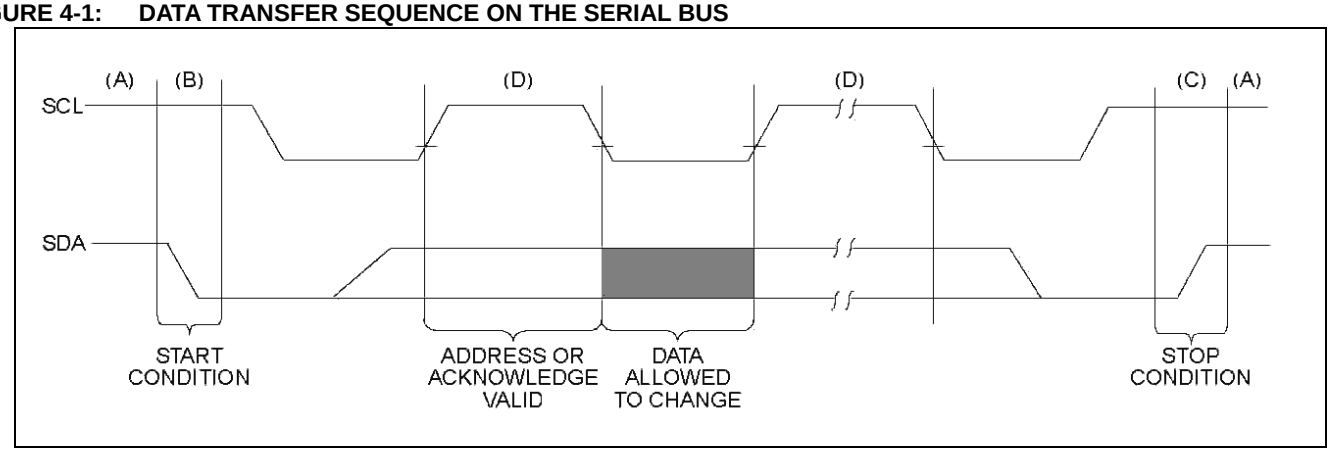
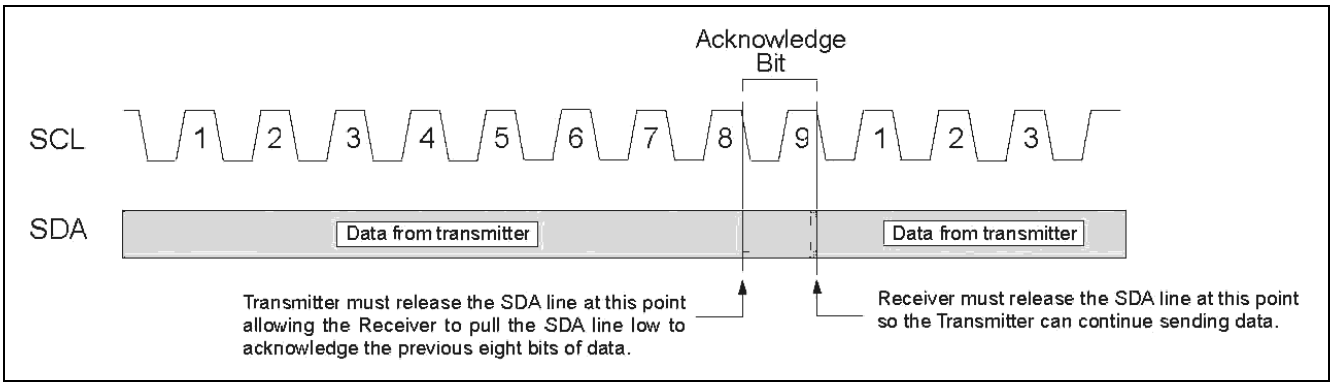


FIGURE 4-2: ACKNOWLEDGE TIMING



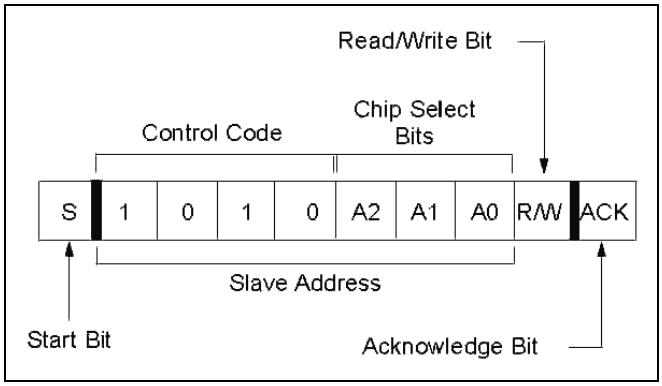
5.0 DEVICE ADDRESSING

A control byte is the first byte received following the start condition from the master device (Figure 5-1). The control byte consists of a four bit control coder; for the 24xx64 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the chip select bit (A2,A1,A0). The chip select bits allow the use of up to eight 24xx64 devices on the same bus and are used to select which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2,A1, and A0 pins for the device to respond. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). Because only A12…A0 are used, the upper three address bits are don't care bits. The upper address bits are transferred first, followed by the less significant bits.

Following the start condition, the 24xx64 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the $\overline{R/W}$ bit, the 24xx64 will select a read or write operation.

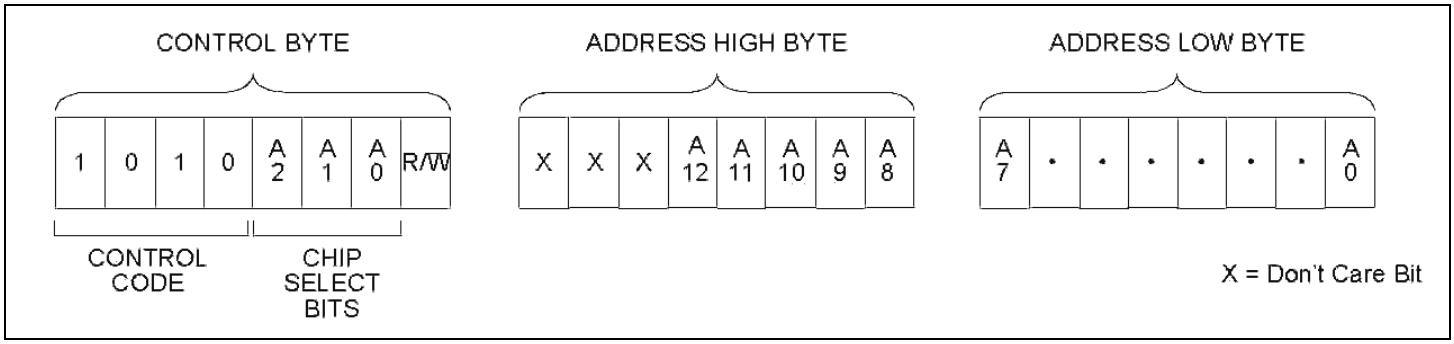
FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The chip select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24xx64's on the same bus. In this case, software can use A0 of the control byte as address bit A13,A1 as address bit A14, and A2 as address bit A15.It is not possible to sequentially read across device boundaries.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start condition from the master, the control code (four bits), the chip select (three bits),and the $\overline{R/W}$ bit (Which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that address high byte will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24xx64. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24xx64 the master device will transmit the data word to be written into the addressed memory location. The 24xx64 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24xx64 will not generate acknowledge signals (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will immediately accept a new command. After a byte write command, the internal address counter will point to the address location following the one that was just written.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24xx64 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 31 additional bytes which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a stop condition. After receipt of each word, the five lower address pointer bits are internally incremented by one. If the master should transmit more than 32 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written and the device will immediately accept a now command.

6.3 Write Protection

The WP pin allows the user to write protect the entire array (0000-1FFF) when the pin is tied to Vcc. If tied to Vss or left floating, the write protection is disabled. The WP pin is sampled at the STOP bit for every write command (Figure 1-1) Toggling the WP pin after the STOP bit will have no effect on the execution of the write cycle.

FIGURE 6-1: BYTE WRITE

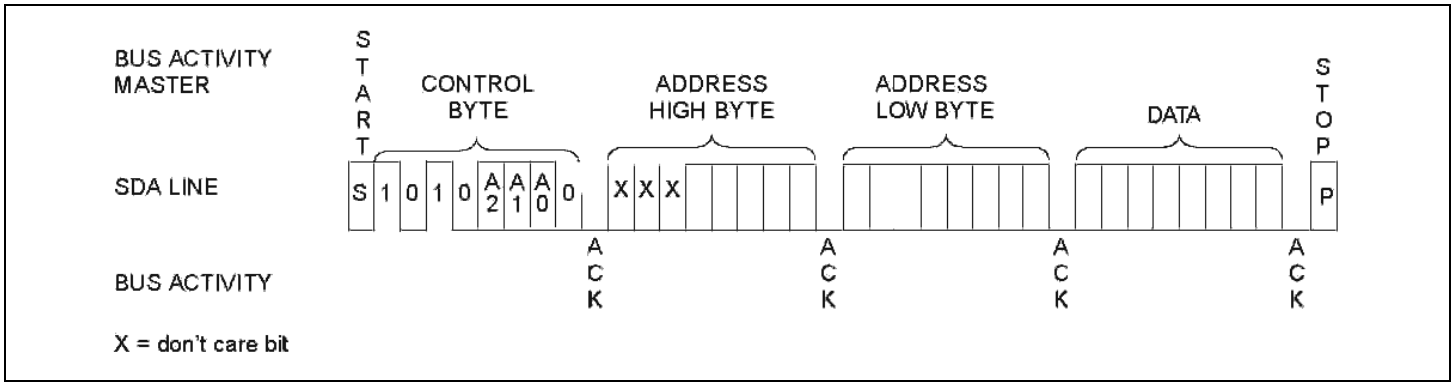
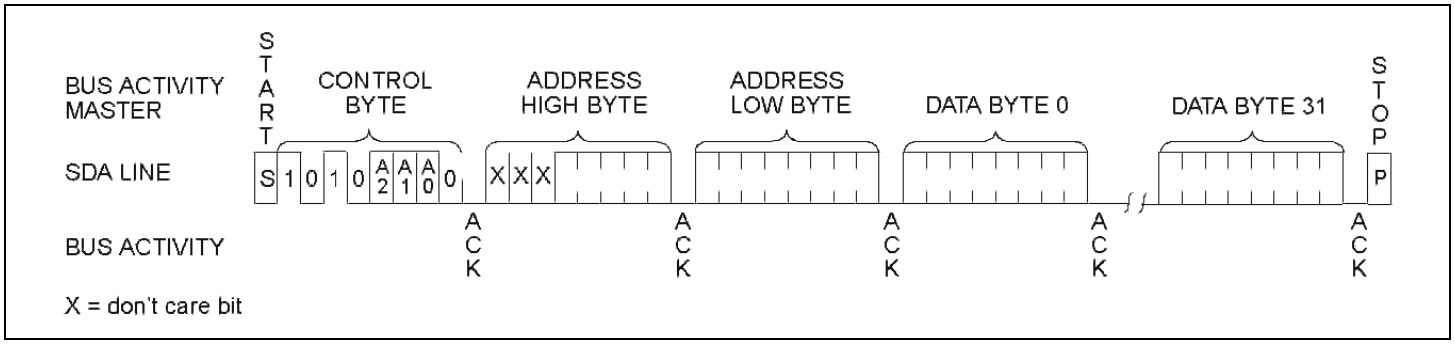


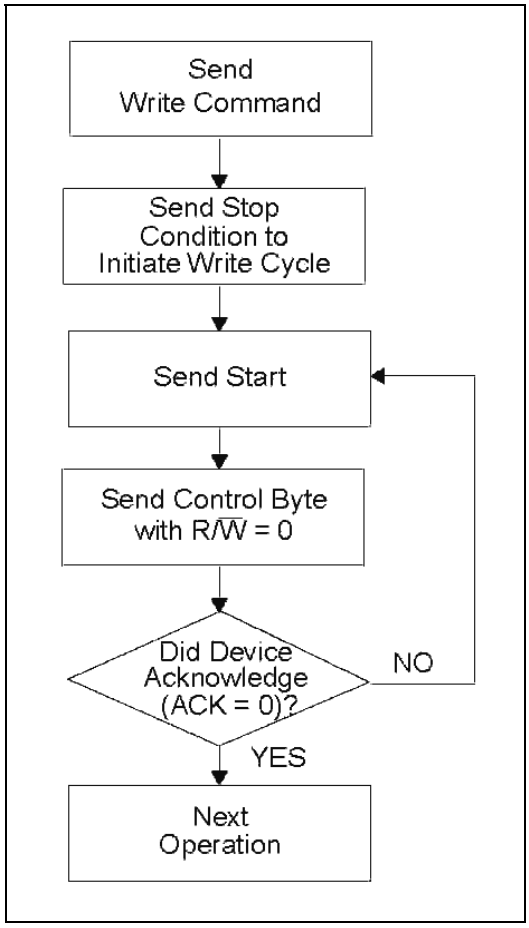
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W}$ =0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

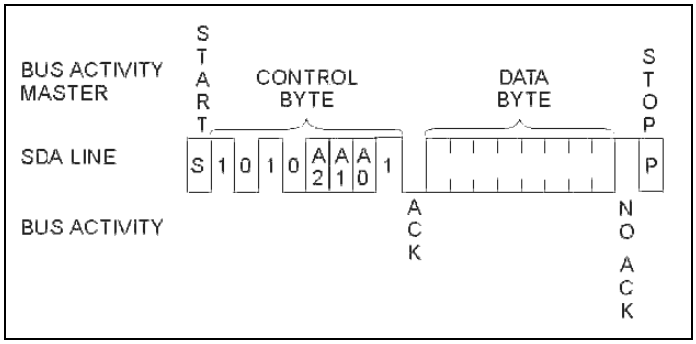
Read operations are initiated in the same way as write operations with the exception that the $R\overline{W}$ bit of the control byte is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24xx64 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n+1.

Upon receipt of the control byte with $R\overline{W}$ bit set to one, the 24xx64 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24xx64 discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24xx64 as part of a write operation ($R\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set, Then the master issues the control byte again but with the $R\overline{W}$ bit set to a one. The 24xx64 will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24xx64 to discontinue transmission (Figure 8-2). After a random read command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24xx64 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24xx64 to transmit the next sequentially addressed 8-bit word (Figure 8-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition. To provide sequential reads the 24xx64 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 1FFF to address 0000 if the master acknowledges the byte received from the array address 1FFF.

FIGURE 8-2: RANDOM READ

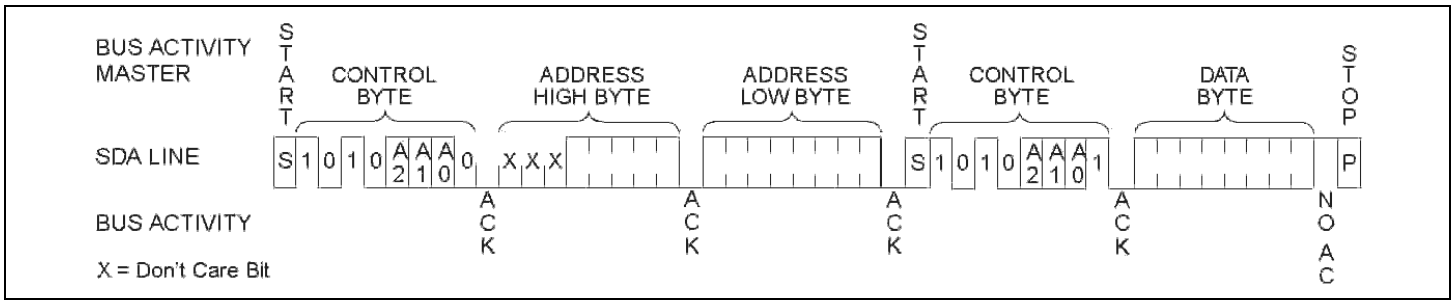
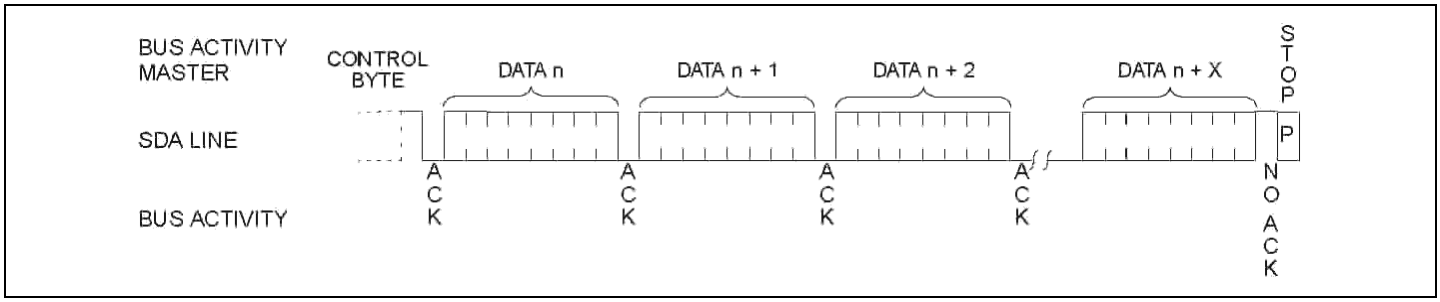


FIGURE 8-3: SEQUENTIAL READ



NOTES:

24xx64 PRODUCT IDENTIFICATION SYSTEM

To order obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.