# 24AA01/02

## 1K/2K 1.8V I²C™ Serial EEPROMs

### FEATURES

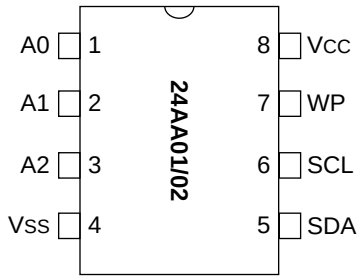
- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 μA standby current typical at 5.5V
  - 3 μA standby current typical at 1.8V
- Organized as a single block of 128 bytes (128 x 8) or 256 bytes (256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- ESD protection > 3,000V
- 10,000,000 ERASE/WRITE cycles guaranteed on 24AA01
- 1,000,000 ERASE/WRITE cycles guaranteed on 24AA02
- Data retention > 200 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I) -40°C to +85°C

### DESCRIPTION

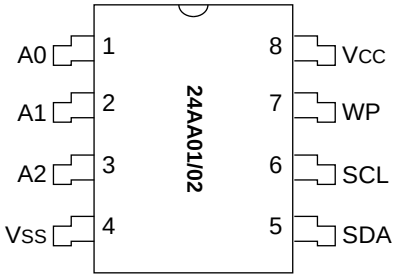
The Microchip Technology Inc. 24AA01 and 24AA02 are 1K bit and 2K bit Electrically Erasable PROMs. The devices are organized as a single block of 128 x 8-bit or 256 x 8-bit memory with a two wire serial interface. Low-voltage design permits operation down to 1.8 volts with standby and active currents of only 3 μA and 1 mA, respectively. The 24AA01 and 24AA02 also have page-write capability for up to 8 bytes of data. The 24AA01 and 24AA02 are available in the standard 8-pin DIP and 8-pin surface mount SOIC packages.

### PACKAGE TYPES

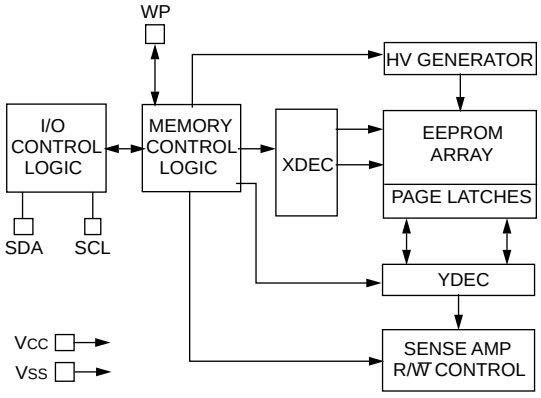
**PDIP**




**SOIC**




### BLOCK DIAGRAM

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## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°CC
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: PIN FUNCTION TABLE**

| Name | Function |
|---|---|
| VSS | Ground |
| SDA | Serial Address/Data/I/O |
| SCL | Serial Clock |
| WP | Write Protect Input |
| VCC | +1.8V to 5.5V Power Supply |
| A0, A1, A2 | No Internal Connection |

**TABLE 1-2: DC CHARACTERISTICS**

| | | | | | | |
|---|---|---|---|---|---|---|
| | VCC = +1.8V to +5.5V<br>Commercial (C): Tamb = 0°C to +70°C<br>Industrial (I): Tamb = -40°C to +85°C | | | | | |
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| WP, SCL and SDA pins: | | | | | | |
| High level input voltage | VIH | .7 VCC | — | — | V | |
| Low level input voltage | VIL | — | — | .3 VCC | V | |
| Hysteresis of Schmitt trigger inputs | VHYS | .05 VDD | — | — | V | (Note) |
| Low level output voltage | VOL | — | — | .40 | V | IOL = 3.0 mA, VCC = 1.8V |
| Input leakage current | ILI | -10 | — | 10 | µA | VIN = .1V to 5.5V |
| Output leakage current | ILO | -10 | — | 10 | µA | VOUT = .1V to 5.5V |
| Pin capacitance (all inputs/outputs) | CIN, COUT | — | — | 10 | pF | Vcc = 5.0V (Note 1)<br>Tamb = 25˚C, FCLK = 1 MHz |
| Operating current | ICC Write | — | — | 3 | mA | VCC = 5.5V, SCL = 400 kHz |
| | | — | 0.5 | — | mA | VCC = 1.8V, SCL = 100 kHz |
| | ICC Read | — | — | 1 | mA | VCC = 5.5V, SCL = 400 kHz |
| | | — | 0.05 | — | mA | VCC = 1.8V, SCL = 100 kHz |
| Standby current | ICCS | — | — | 100 | µA | VCC = 5.5V, SDA = SCL = VCC |
| | | — | — | 30 | µA | VCC = 3.0V, SDA = SCL = VCC |
| | | — | 3 | — | µA | VCC = 1.8V, SDA = SCL = VCC |

Note:This parameter is periodically sampled and not 100% tested.

**FIGURE 1-1: BUS TIMING START/STOP**

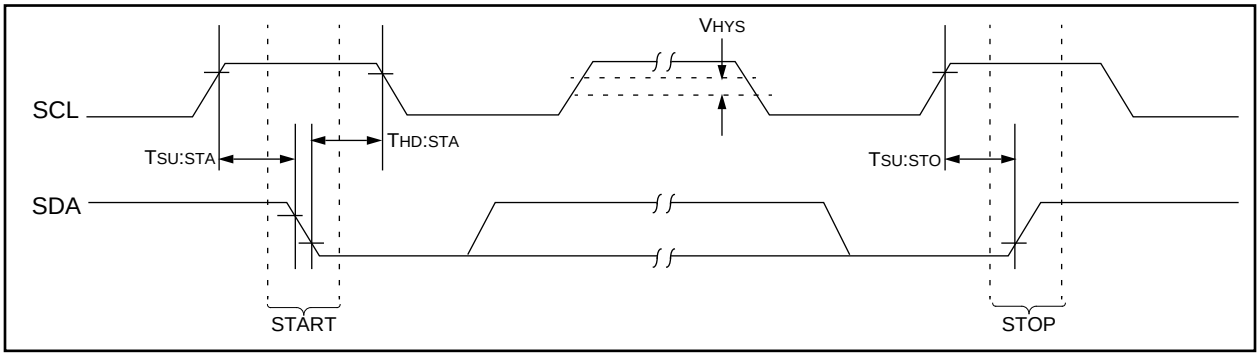



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**TABLE 1-3: AC CHARACTERISTICS**

| Parameter | Symbol | Standard Mode | | $V_{CC}$ = 4.5 - 5.5V Fast Mode | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Clock frequency | Fclk | — | 100 | — | 400 | kHz | |
| Clock high time | Thigh | 4000 | — | 600 | — | ns | |
| Clock low time | Tlow | 4700 | — | 1300 | — | ns | |
| SDA and SCL rise time | Tr | — | 1000 | — | 300 | ns | (Note 1) |
| SDA and SCL fall time | Tf | — | 300 | — | 300 | ns | (Note 1) |
| START condition hold time | Thd:sta | 4000 | — | 600 | — | ns | After this period the first clock pulse is generated |
| START condition setup time | Tsu:sta | 4700 | — | 600 | — | ns | Only relevant for repeated START condition |
| Data input hold time | Thd:dat | 0 | — | 0 | — | ns | (Note 2) |
| Data input setup time | Tsu:dat | 250 | — | 100 | — | ns | |
| STOP condition setup time | Tsu:sto | 4000 | — | 600 | — | ns | |
| Output valid from clock | Taa | — | 3500 | — | 900 | ns | (Note2) |
| Bus free time | Tbuf | 4700 | — | 1300 | — | ns | Time the bus must be free before a new transmission can start |
| Output fall time from $V_{IH}$ min to $V_{IL}$ max | Tof | — | 250 | 20 +0.1 $C_B$ | 250 | ns | (Note 1), $C_B \leq 100$ pF |
| Input filter spike suppression (SDA and SCL pins) | $T_{SP}$ | — | 50 | — | 50 | ns | (Note 3) |
| Write cycle time | Twr | — | 10 | — | 10 | ms | Byte or Page mode |
| Endurance 24AA01<br>24AA02 | — | 10M<br>1M | — | 10M<br>1M | — | cycles | 25°C, Vcc = 5.5V, Block Mode (Note 4) |

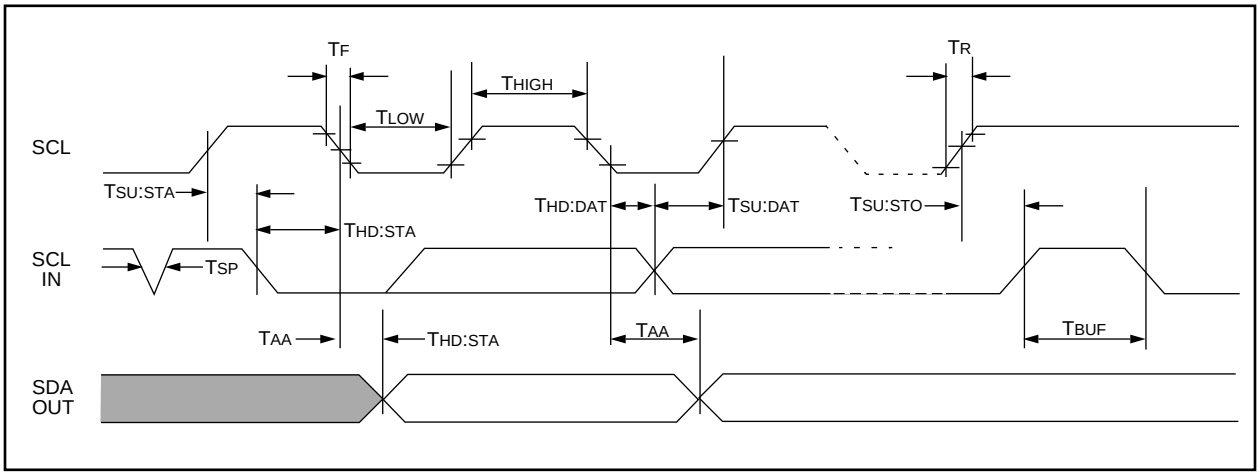
Note 1: Not 100% tested. $C_B$ = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined $T_{SP}$ and $V_{HYS}$ specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a $T_I$ specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

**FIGURE 1-2: BUS TIMING DATA**



## 2.0 FUNCTIONAL DESCRIPTION

The 24AA01/02 supports a bi directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA01/02 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

## 3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

### 3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

### 3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

### 3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

### 3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

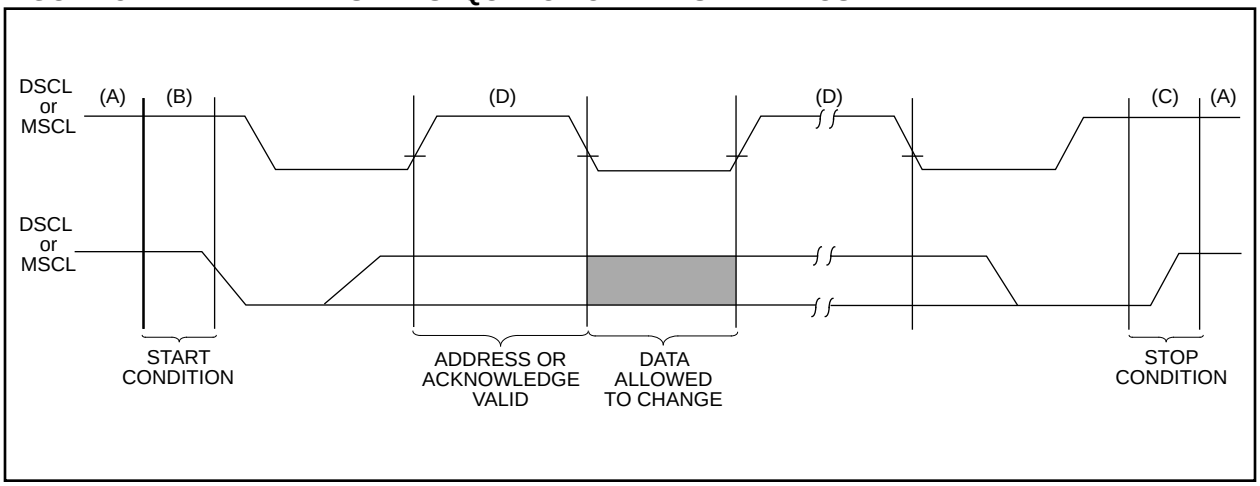
### 3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

| | |
|---|---|
| **Note:** | The 24AA01/02 does not generate any acknowledge bits if an internal programming cycle is in progress. |

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

**FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS**





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### 3.6 Device Address

The 24AA01/02 are software-compatible with older devices such as 24C01A, 24C02A, 24LC01, and 24LC02. A single 24AA02 can be used in place of two 24LC01's, for example, without any modifications to software. The “chip select” portion of the control byte becomes a don't care.

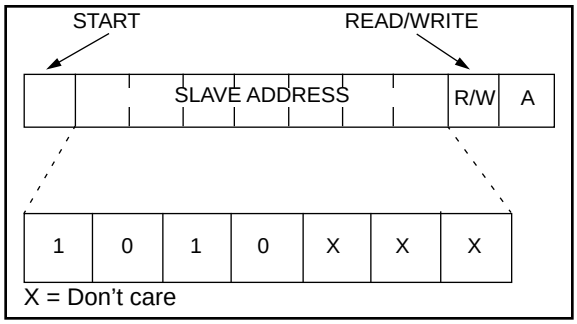
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24AA01/02, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24AA01/02 (Figure 3-2).

The 24AA01/02 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

| Operation | Control Code | Chip Select | R/$\overline{W}$ |
|---|---|---|---|
| Read | 1010 | XXX | 1 |
| Write | 1010 | XXX | 0 |

**FIGURE 3-2: CONTROL BYTE ALLOCATION**




## 4.0 WRITE OPERATION

### 4.1 Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA01/02. After receiving another acknowledge signal from the 24AA01/02 the master device will transmit the data word to be written into the addressed memory location. The 24AA01/02 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA01/02 will not generate acknowledge signals (Figure 4-1).

### 4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA01/02 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24AA01/02 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 7-1).

**FIGURE 4-1: BYTE WRITE**

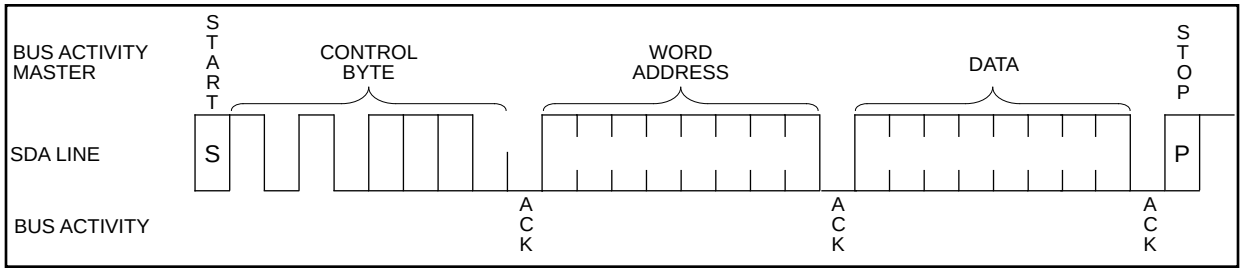
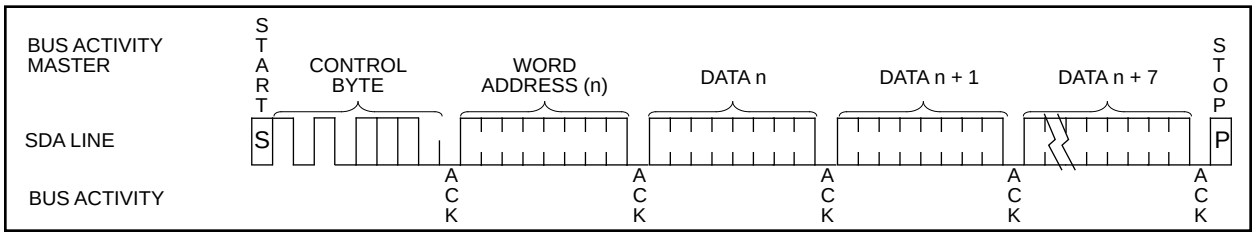


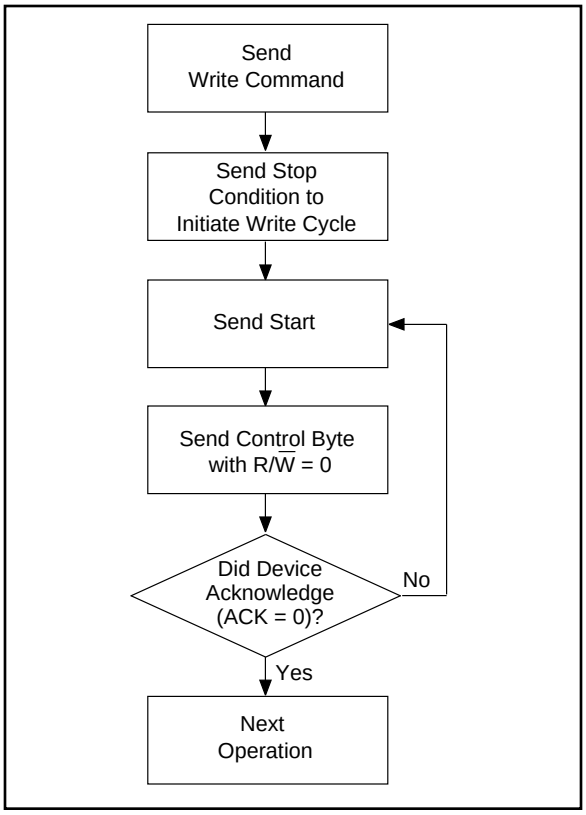

**FIGURE 4-2: PAGE WRITE**



## 5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

**FIGURE 5-1: ACKNOWLEDGE POLLING FLOW**




## 6.0 WRITE PROTECTION

The 24AA01/02 can be used as a serial ROM when the WP pin is connected to VCC. Programming will be inhibited and the entire memory will be write-protected.

## 7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

### 7.1 Current Address Read

The 24AA01/02 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA01/02 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA01/02 discontinues transmission (Figure 7-1).

### 7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA01/02 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA01/02 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA01/02 discontinues transmission (Figure 7-2).

### 7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA01/02 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA01/02 to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24AA01/02 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

### 7.4 Noise Protection

The 24AA01/02 employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.


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**FIGURE 7-1: CURRENT ADDRESS READ**

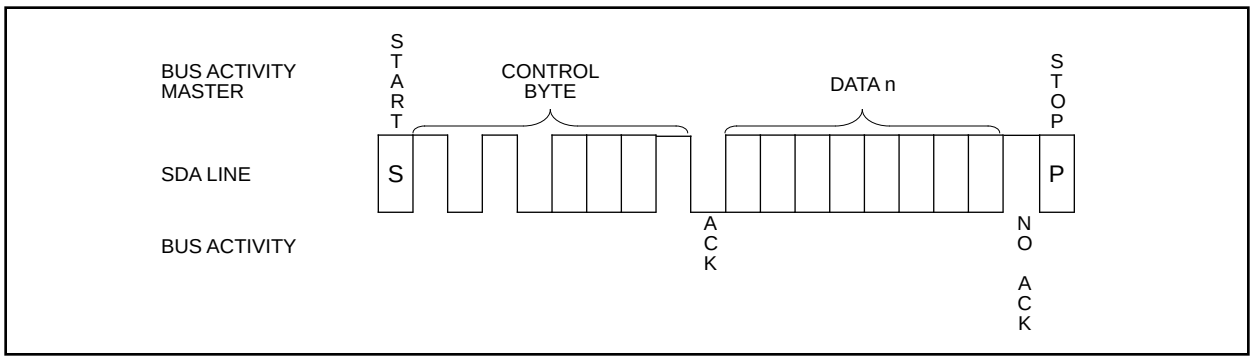



**FIGURE 7-2: RANDOM READ**

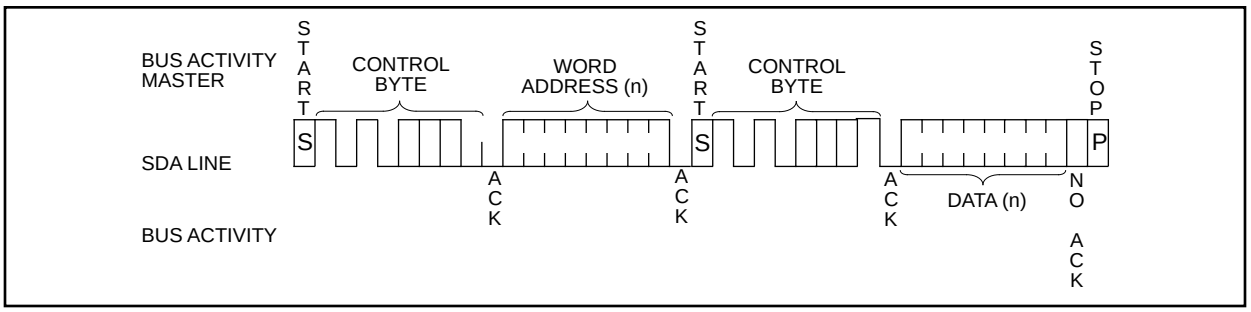
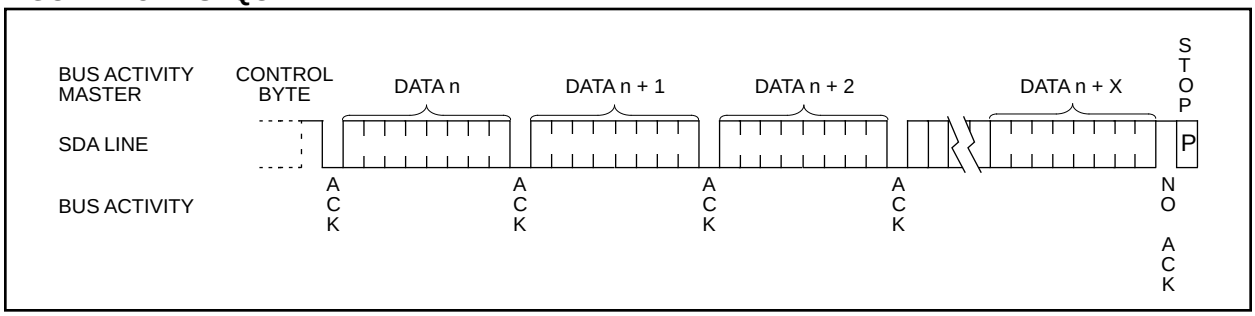



**FIGURE 7-3: SEQUENTIAL READ**




## 8.0 PIN DESCRIPTIONS

### 8.1 SDA Serial Address/Data Input/Output

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 1K for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

### 8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

### 8.3 WP

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory).

If tied to VCC, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA01/02 as a serial ROM when WP is enabled (tied to VCC).

### 8.4 A0, A1, A2

These pins are not used by the 24AA01/02. They may be left floating or tied to either VSS or VCC.

**NOTES:**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**NOTES:**

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## 24AA01/02 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.

**24AA01/02 - /P**

| | | | |
|---|---|---|---|
| **Package:** | P | = | Plastic DIP (300 mil Body), 8-lead |
| | SN | = | Plastic SOIC (150 mil Body), 8-lead |
| | SM | = | Plastic SOIC (207 mil Body), 8-lead |
| **Temperature Range:** | Blank | = | 0°C to +70°C |
| | I | = | -40°C to +85°C |
| **Device:** | 24AA01 | | 1.8V, 1K $I^2C$ Serial EEPROM |
| | 24AA01T | | 1.8V, 1K $I^2C$ Serial EEPROM (Tape and Reel) |
| | 24AA02 | | 1.8V, 2K $I^2C$ Serial EEPROM |
| | 24AA02T | | 1.8V, 2K $I^2C$ Serial EEPROM (Tape and Reel) |

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