TMC 24A01/24A02/24A04/24A08/24A16

1K/2K/4K/8K/16K-bit
Serial EEPROM for Low Power

Data Sheet

OVERVIEW

The TMC 24A01/24A02/24A04/24A08/24A16 serial EEPROM has a 1,024/2,048/4,096/8,192/16,384-bit capacity, supporting the standard I^{2}C™-bus serial interface. It is fabricated using TMC's most advanced CMOS technology. It has been developed for low power and low voltage applications (1.8 V to 5.5 V). One of its major feature is a hardware-based write protection circuit for the entire memory area. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. Using one-page write mode, you can load up to 16 bytes of data into the EEPROM in a single write operation. Another significant feature of the TMC 24A01/24A02/24A08/24A16 is its support for fast mode and standard mode.

FEATURES

I^{2}C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

- 1K/2K/4K/8K/16K-bit (128/256/512/1,024/2,048-byte) storage area
- 16-byte page buffer
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- EEPROM programming voltage generated on chip
- 1,000,000 erase/write cycles
- 100 years data retention
- 24AXXL Marking means Lead Free product
- 24AXXG Marking means Green product

Operating Characteristics

- Operating voltage
  - 1.8 V to 5.5 V
- Operating current
  - Maximum write current: < 3 mA at 5.5 V
  - Maximum read current: < 200 µA at 5.5 V
  - Maximum stand-by current: < 5 µA at 5.5 V
- Operating temperature range
  - – 25°C to + 70°C (commercial)
  - – 40°C to + 85°C (industrial)
- Operating clock frequencies
  - 100 kHz at standard mode
  - 400 kHz at fast mode
- Electrostatic discharge (ESD)
  - 5,000 V (HBM)
  - 500 V (MM)

Packages

- 8-pin DIP, SOP, TSSOP, and SOT 25

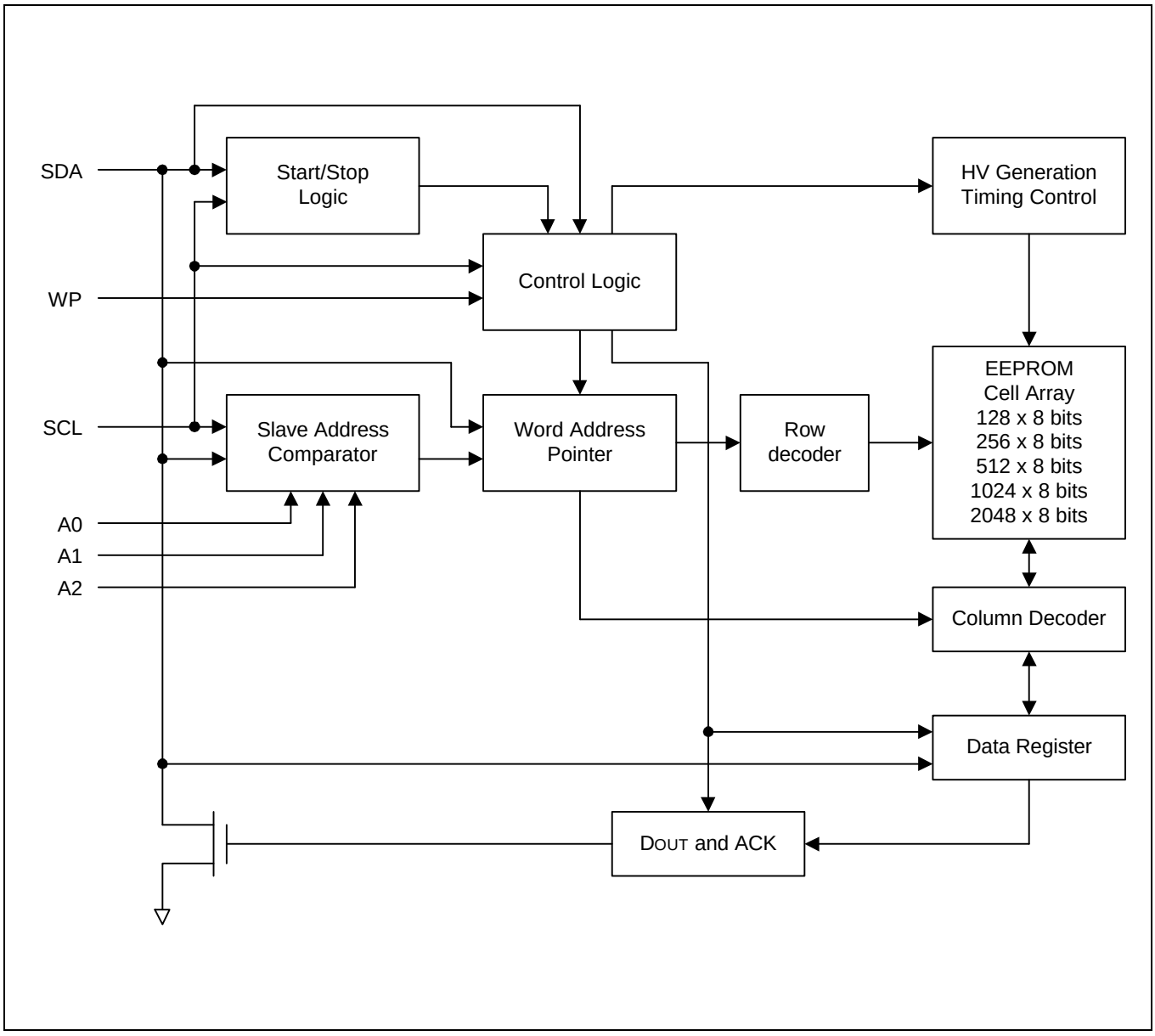
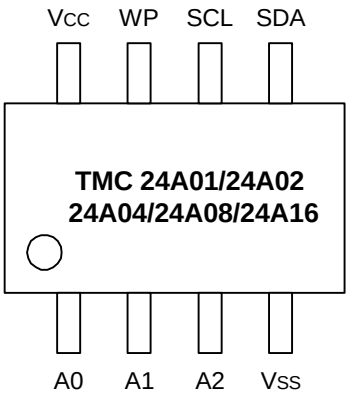
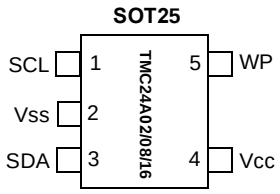


Figure 3-1. Block Diagram





NOTE: The TMC 24A01/24A02/24A04/24A08/24A16 is available in 8-pin DIP, SOP, TSSOP, and SOT 25 package.

Figure 3-2. Pin Assignment Diagram

Table 3-1. Pin Descriptions

Name	Type	Description	Circuit Type
A0, A1, A2	Input	Input pins for device address selection. To configure a device address, these pins should be connected to the V_{CC} or V_{SS} of the device. These pins are internally pulled down to V_{SS}.	1
V_{SS}	–	Ground pin.	–
SDA	I/O	Bi-directional data pin for the I^2C-bus serial data interface. Schmitt trigger input and open-drain output. An external pull-up resistor must be connected to $V_{CC.}$ Typical values for this pull-up resistor are 4.7 kΩ (100 kHz) and 1 kΩ (400 kHz).	3
SCL	Input	Schmitt trigger input pin for serial clock input.	2
WP	Input	Input pin for hardware write protection control. If you tie this pin to $V_{CC,}$ the write function is disabled to protect previously written data in the entire memory; if you tie it to V_{SS}, the write function is enabled. This pin is internally pulled down to V_{SS}.	1
V_{CC}	–	Single power supply.	–

NOTE: See the following page for diagrams of pin circuit types 1, 2, and 3.

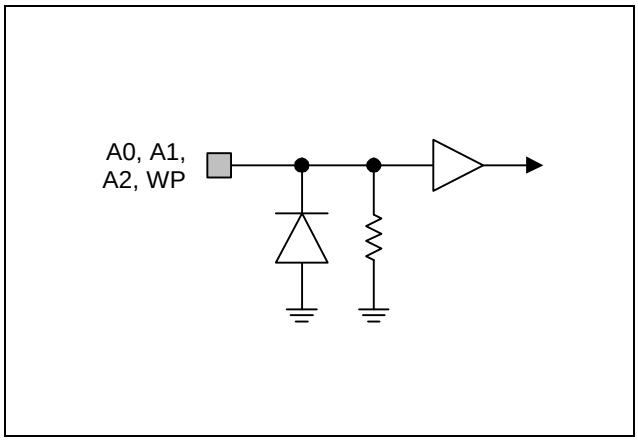


Figure 3-3. Pin Circuit Type 1

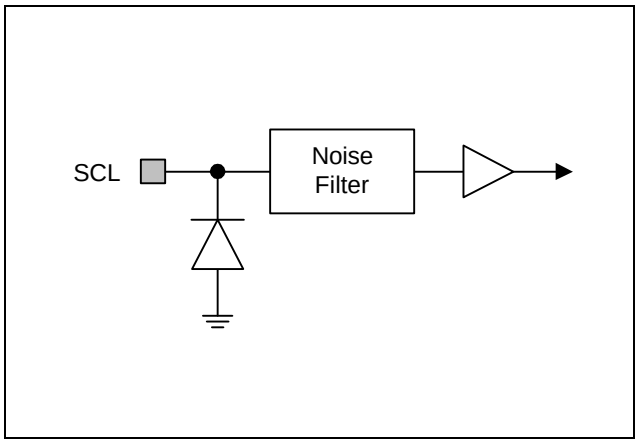


Figure 3-4. Pin Circuit Type 2

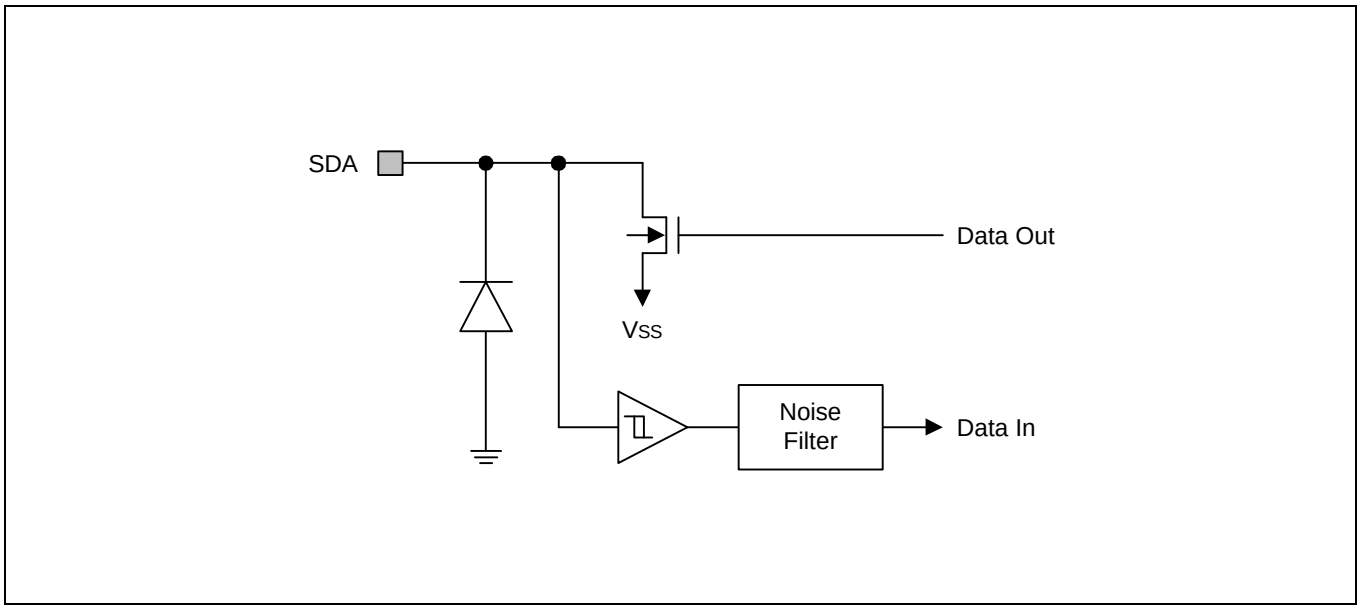


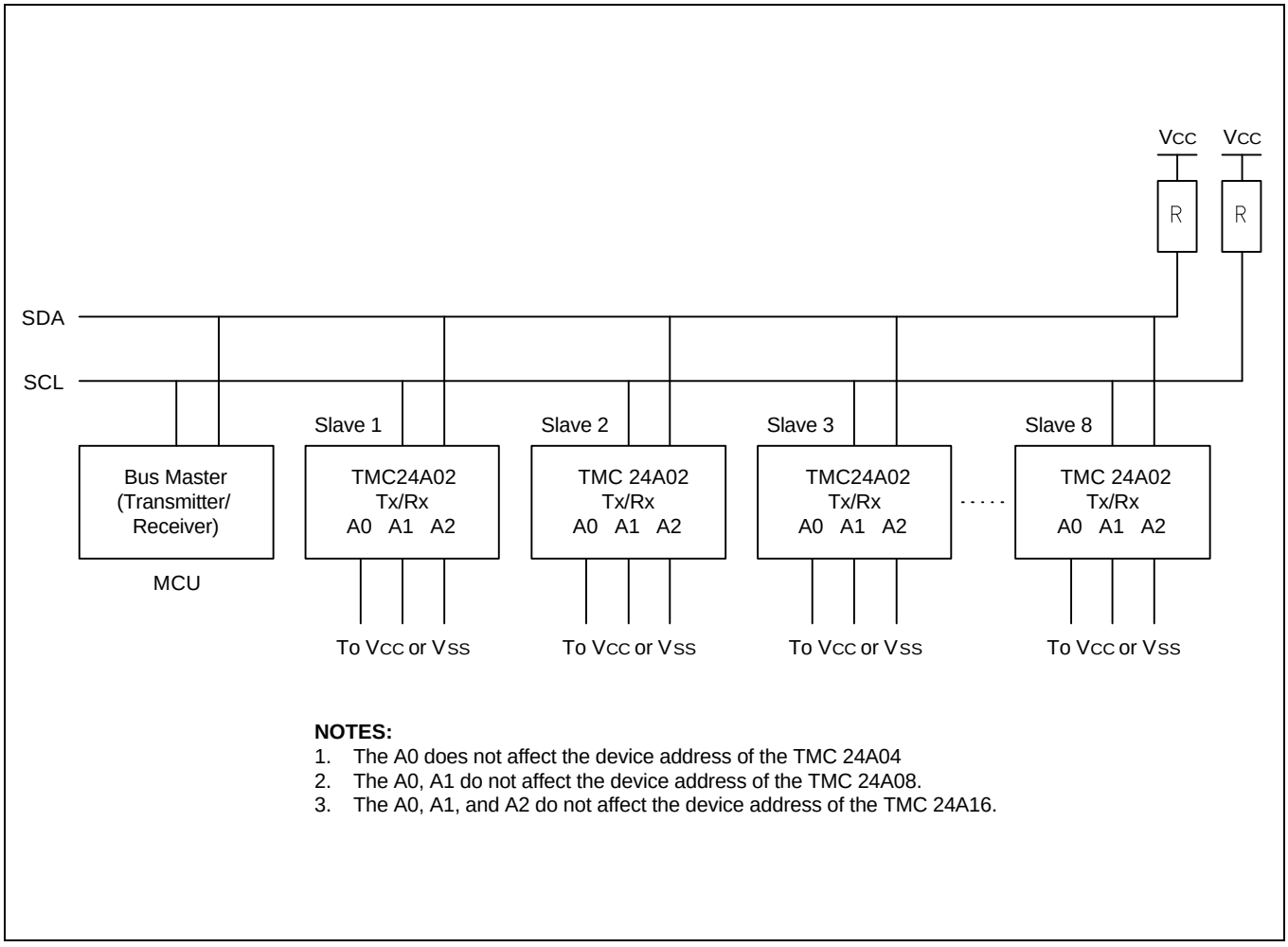
Figure 3-5. Pin Circuit Type 3

FUNCTION DESCRIPTION

I²C-BUS INTERFACE

The TMC 24A01/24A02/24A04/24A08/24A16 supports the I²C-bus serial interface data transmission protocol. The two-wire bus consists of a serial data line (SDA) and a serial clock line (SCL). The SDA and the SCL lines must be connected to V_{CC} by a pull-up resistor that is located somewhere on the bus.

Any device that puts data onto the bus is defined as the “transmitter” and any device that gets data from the bus is the “receiver.” The bus is controlled by a master device which generates the serial clock and start/stop conditions, controlling bus access. Using the A0, A1, and A2 input pins, up to eight TMC 24A01/24A02 (four TMC24A04, two for TMC24A08, one for TMC24A16) devices can be connected to the same I²C-bus as slaves (see Figure 3-6). Both the master and slaves can operate as transmitter or receiver, but the master device determines which bus operating mode would be active.



NOTES:
1. The A0 does not affect the device address of the TMC 24A04
2. The A0, A1 do not affect the device address of the TMC 24A08.
3. The A0, A1, and A2 do not affect the device address of the TMC 24A16.

Figure 3-6. Typical Configuration (16 Kbits of Memory on the I²C-Bus)

I²C-BUS PROTOCOLS

Here are several rules for I²C-bus transfers:

— A new data transfer can be initiated only when the bus is currently not busy.

— MSB is always transferred first in transmitting data.

— During a data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is High.

The I²C-bus interface supports the following communication protocols:

- Bus not busy: The SDA and the SCL lines remain High level when the bus is not active.
- Start condition: Start condition is initiated by a High-to-Low transition of the SDA line while SCL remains High level. All bus commands must be preceded by a start condition.
- Stop condition: A stop condition is initiated by a Low-to-High transition of the SDA line while SCL remains High level. All bus operations must be completed by a stop condition (see Figure 3-7).

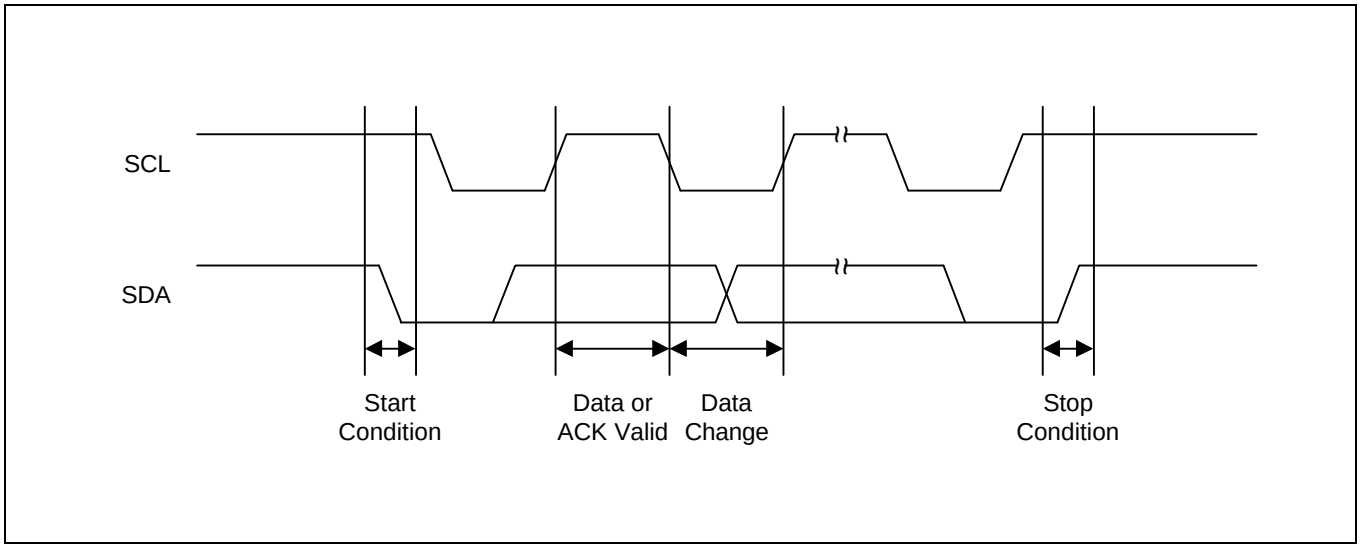


Figure 3-7. Data Transmission Sequence

- Data valid: Following a start condition, the data becomes valid if the data line remains stable for the duration of the High period of SCL. New data must be put onto the bus while SCL is Low. Bus timing is one clock pulse per data bit. The number of data bytes to be transferred is determined by the master device. The total number of bytes that can be transferred in one operation is theoretically unlimited.
- ACK (Acknowledge): An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the 9th clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it successfully received the eight bits of data (see Figure 3-8). But the slave does not send an ACK if an internal write cycle is still in progress.

  In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the 9th clock period. If an ACK is detected, the slave will continue to transmit data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.

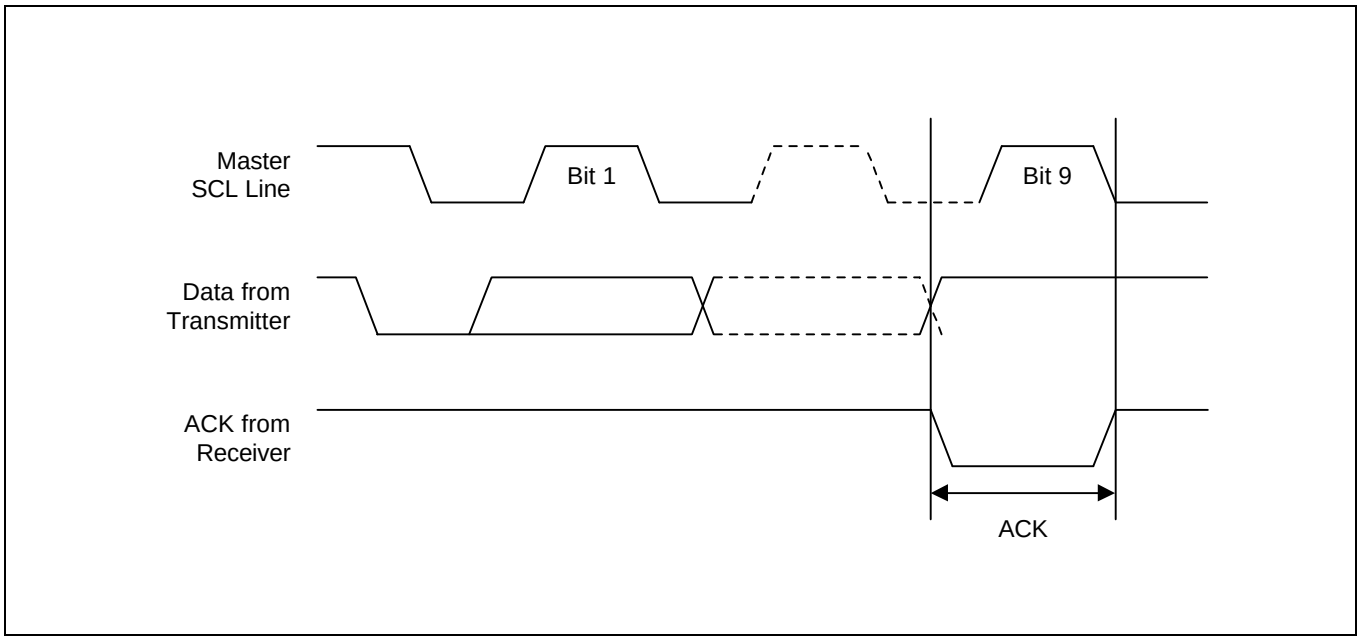


Figure 3-8. Acknowledge Response From Receiver

- Slave Address: After the master initiates a Start condition, it must output the address of the device to be accessed. The most significant four bits of the slave address are called the “device identifier”. The identifier for the TMC 24A01/24A02/24A04/24A08/24A16 is “1010B”. The next three bits comprise the address of a specific device. The device address is defined by the state of the A0, A1 and A2 pins. Using this addressing scheme, you can cascade up to eight TMC 24A01/24A02 or four TMC 24A04 or two TMC 24A08 or one TMC 24A16 on the bus (see Table 3-2 below). The b1 for TMC 24A04 or the b1, b2 for TMC 24A08 or the b1, b2, b3 for TMC24A16 are used by the master to select which of the blocks of internal memory (1 block = 256 words) are to be accessed. The bits are in effect the most significant bits of the word address.
- Read/Write: The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is “1”, a read operation is executed. If it is “0”, a write operation is executed.

Table 3-2. Slave Device Addressing

Device	Device Identifier				Device Address			R/W Bit
	b7	b6	b5	b4	b3	b2	b1	b0
TMC24A01/24A02	1	0	1	0	A2	A1	A0	R/W
TMC24A04	1	0	1	0	A2	A1	B0	R/W
TMC24A08	1	0	1	0	A2	B1	B0	R/W
TMC24A16	1	0	1	0	B2	B1	B0	R/W

NOTE: The B2, B1, B0 correspond to the MSB of the memory array address word.

BYTE WRITE OPERATION

In a complete byte write operation, the master transmits the slave address, word address, and one data byte to the TMC 24A01/24A02/24A04/24A08/24A16 slave device (see Figure 3-9).

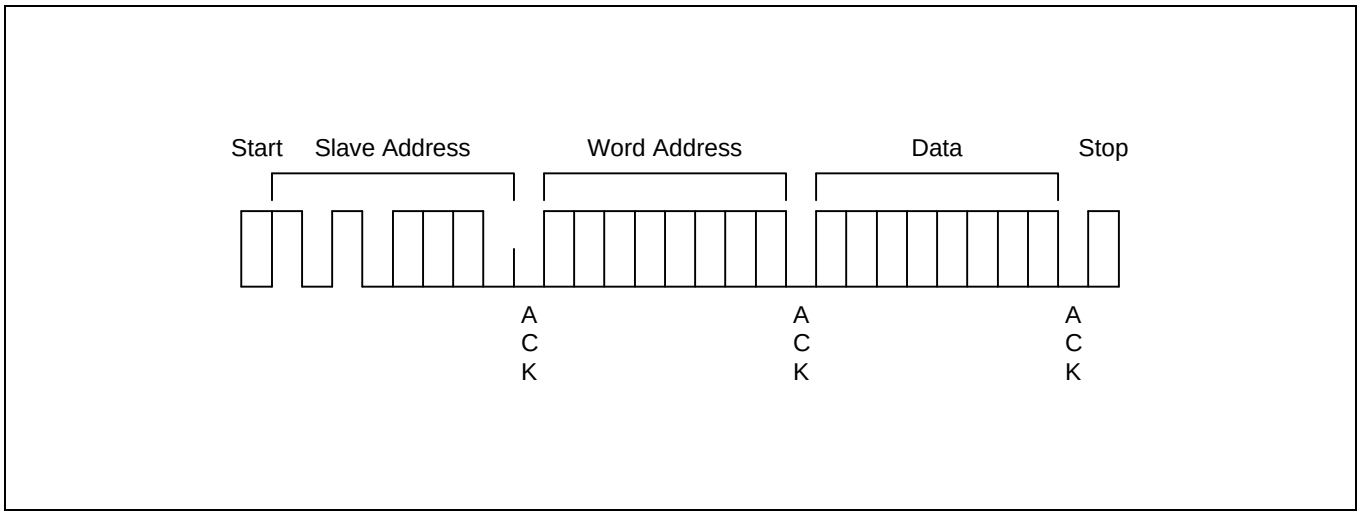


Figure 3-9. Byte Write Operation

Following the Start condition, the master sends the device identifier (4 bits), the device address (3 bits), and an R/W bit set to “0” onto the bus. Then the addressed TMC 24A01/24A02/24A04/24A08/24A16 generates an ACK and waits for the next byte. The next byte to be transmitted by the master is the word address. This 8-bit address is written into the word address pointer of the TMC 24A01/24A02/24A04/24A08/24A16.

When the TMC 24A01/24A02/24A04/24A08/24A16 receives the word address, it responds by issuing an ACK and then waits for the next 8-bit data. When it receives the data byte, the TMC 24A01/24A02/24A04/24A08/24A16 again responds with an ACK. The master terminates the transfer by generating a Stop condition, at which time the TMC 24A01/24A02/24A04/24A08/24A16 begins the internal write cycle.

While the internal write cycle is in progress, all TMC 24A01/24A02/24A04/24A08/24A16 inputs are disabled and the TMC 24A01/24A02/24A04/24A08/24A16 does not respond to additional requests from the master.

PAGE WRITE OPERATION

The TMC 24A01/24A02/24A04/24A08/24A16 can also perform 16-byte page write operation. A page write operation is initiated in the same way as a byte write operation. However, instead of finishing the write operation after the first data byte is transferred, the master can transmit up to 15 additional bytes. The TMC 24A01/24A02/24A04/24A08/24A16 responds with an ACK each time it receives a complete byte of data (see Figure 3-10).

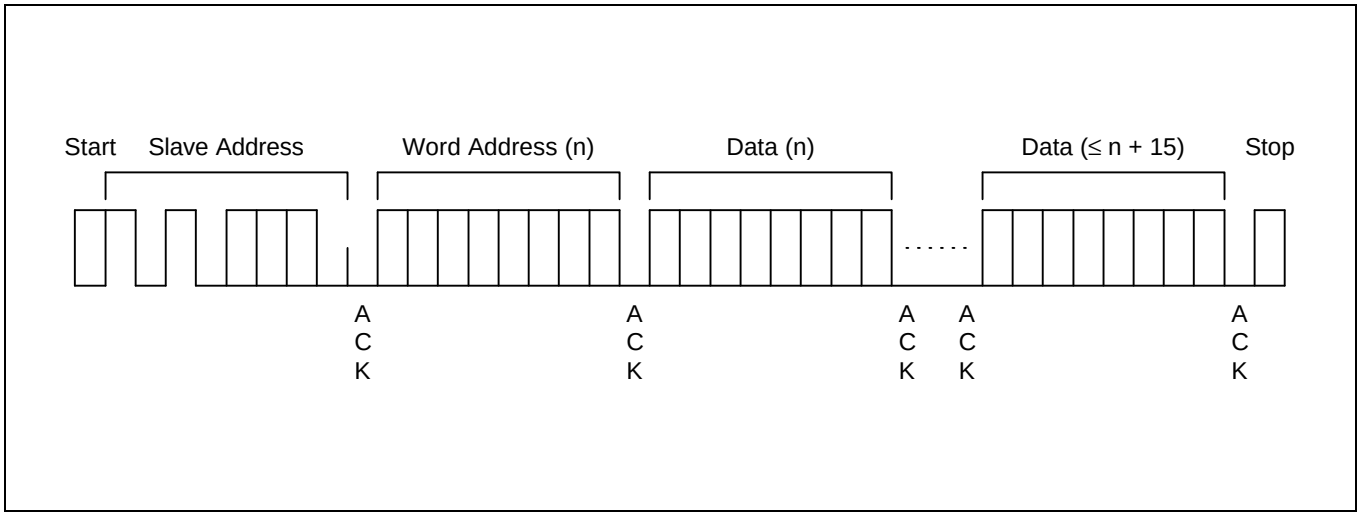


Figure 3-10. Page Write Operation

The TMC 24A01/24A02/24A04/24A08/24A16 automatically increments the word address pointer each time it receives a complete data byte. When one byte has been received, the internal word address pointer increments to the next address and the next data byte can be received.

If the master transmits more than 16 bytes before it generates a stop condition to end the page write operation, the TMC 24A01/24A02/24A04/24A08/24A16 word address pointer value “rolls over” and the previously received data is overwritten. If the master transmits less than 16 bytes and generates a stop condition, the TMC 24A01/24A02/24A04/24A08/24A16 writes the received data to the corresponding EEPROM address.

During a page write operation, all inputs are disabled and there is no response to additional requests from the master until the internal write cycle is completed.

POLLING FOR AN ACK SIGNAL

When the master issues a stop condition to initiate a write cycle, the TMC 24A01/24A02/24A04/24A08/24A16 starts an internal write cycle. The master can then immediately begin polling for an ACK from the slave device.

To poll for an ACK signal in a write operation, the master issues a start condition followed by the slave address. As long as the TMC 24A01/24A02/24A04/24A08/24A16 remains busy with the write operation, no ACK is returned. When the TMC 24A01/24A02/24A04/24A08/24A16 completes the write operation, it returns an ACK and the master can then proceed with the next read or write operation (see Figure 3-11).

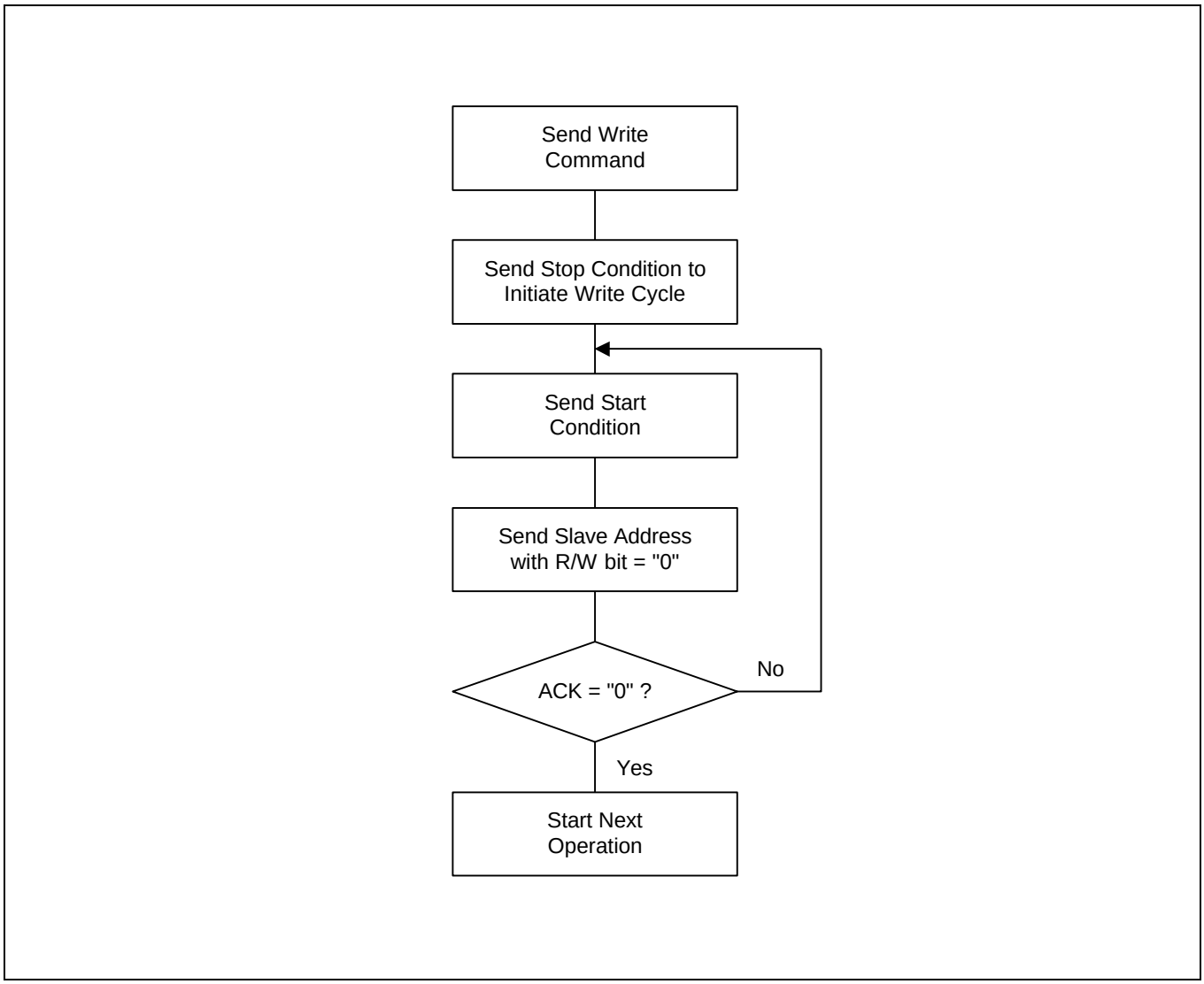


Figure 3-11. Master Polling for an ACK Signal from a Slave Device

HARDWARE-BASED WRITE PROTECTION

You can also write-protect the entire memory area of the TMC 24A01/24A02/24A04/24A08/24A16. This method of write protection is controlled by the state of the Write Protect (WP) pin.

When the WP pin is connected to V_{CC}, any attempt to write a value to the memory is ignored.
The TMC 24A01/24A02/24A04/24A08/24A16 will acknowledge slave and word address, but it will not generate an acknowledge after receiving the first byte of the data. Thus the write cycle will not be started when the stop condition is generated. By connecting the WP pin to V_{SS}, the write function is allowed for the entire memory.

These write protection features effectively change the EEPROM to a ROM in order to prevent data from being overwritten. Whenever the write function is disabled, a slave address and a word address are acknowledged on the bus, but data bytes are not acknowledged.

CURRENT ADDRESS BYTE READ OPERATION

The internal word address pointer maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either read or write) was to the address “n”, the next read operation would access data at address “n+1”.

When the TMC 24A01/24A02/24A04/24A08/24A16receives a slave address with the R/W bit set to “1”, it issues an ACK and sends the eight bits of data. The master does not acknowledge the transfer but it does generate a Stop condition. In this way, the TMC 24A01/24A02/24A04/24A08/24A16 effectively stops the transmission (see Figure 3-12).

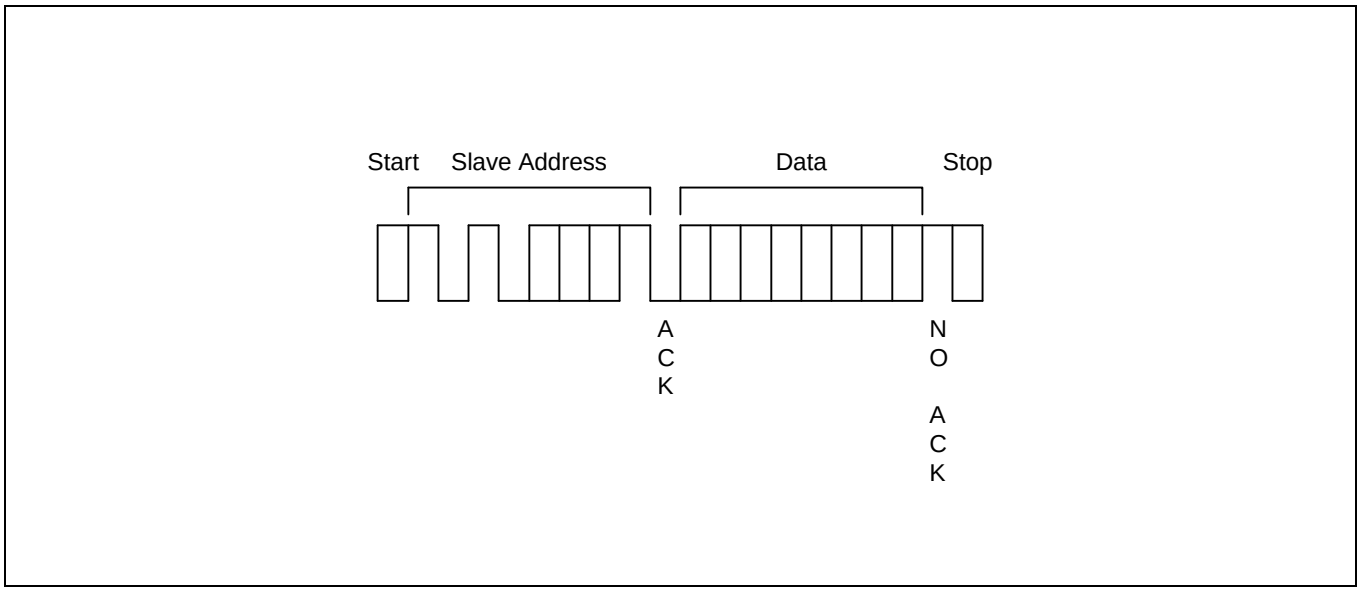


Figure 3-12. Current Address Byte Read Operation

RANDOM ADDRESS BYTE READ OPERATION

Using random read operations, the master can access any memory location at any time. Before it issues the slave address with the R/W bit set to “1”, the master must first perform a “dummy” write operation. This operation is performed in the following steps:

1. The master first issues a Start condition, the slave address, and the word address to be read. (This step sets the internal word address pointer of the TMC 24A01/24A02/24A04/24A08/24A16 to the desired address.)
2. When the master receives an ACK for the word address, it immediately re-issues a start condition followed by another slave address, with the R/W bit set to “1”.
3. The TMC 24A01/24A02/24A04/24A08/24A16 then sends an ACK and the 8-bit data stored at the desired address.
4. At this point, the master does not acknowledge the transmission, but generates a stop condition instead.
5. In response, the TMC 24A01/24A02/24A04/24A08/24A16 stops transmitting data and reverts to its stand-by mode (see Figure 3-13).

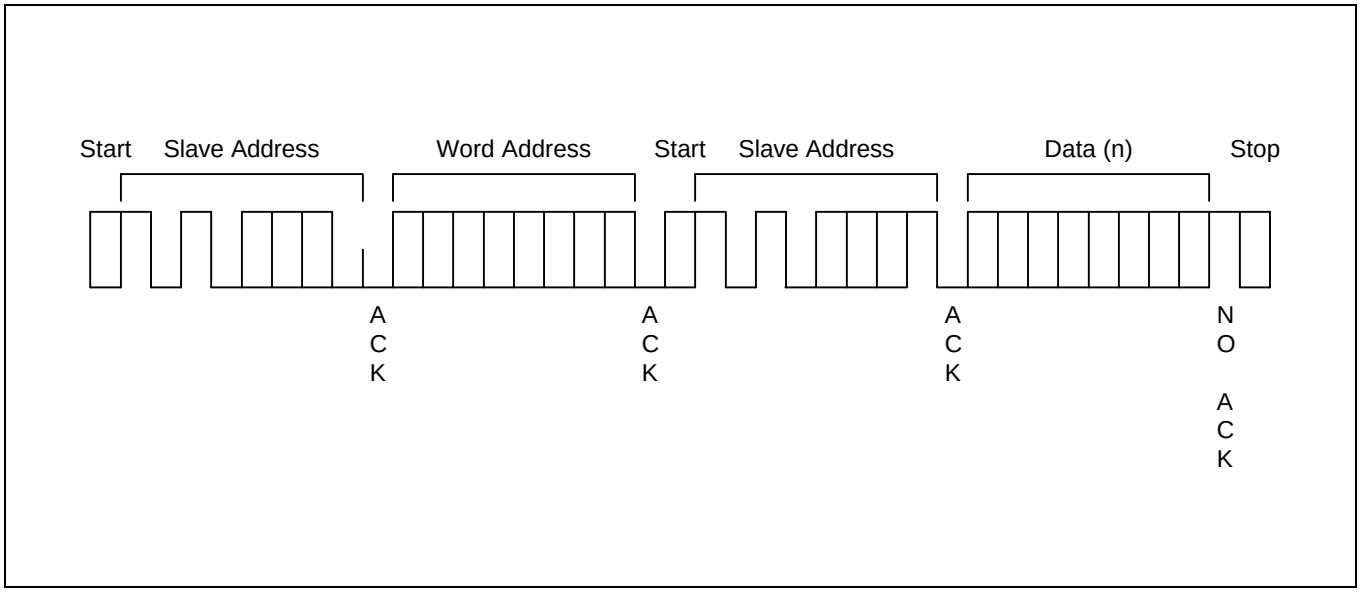


Figure 3-13. Random Address Byte Read Operation

SEQUENTIAL READ OPERATION

Sequential read operations can be performed in two ways: as a series of current address reads or as random address reads. The first data is sent in the same way as the previous read mode used on the bus. The next time, however, the master responds with an ACK, indicating that it requires additional data.
The TMC 24A01/24A02/24A04/24A08/24A16 continues to output data for each ACK it receives. To stop the sequential read operation, the master does not respond with an ACK, but instead issues a Stop condition.

Using this method, data is output sequentially with the data from address “n” followed by the data from “n+1”. The word address pointer for read operations increments all word addresses, allowing the entire EEPROM to be read sequentially in a single operation. After the entire EEPROM is read, the word address pointer “rolls over” and the TMC 24A01/24A02/24A04/24A08/24A16 continues to transmit data for each ACK it receives from the master (see Figure 3-14).

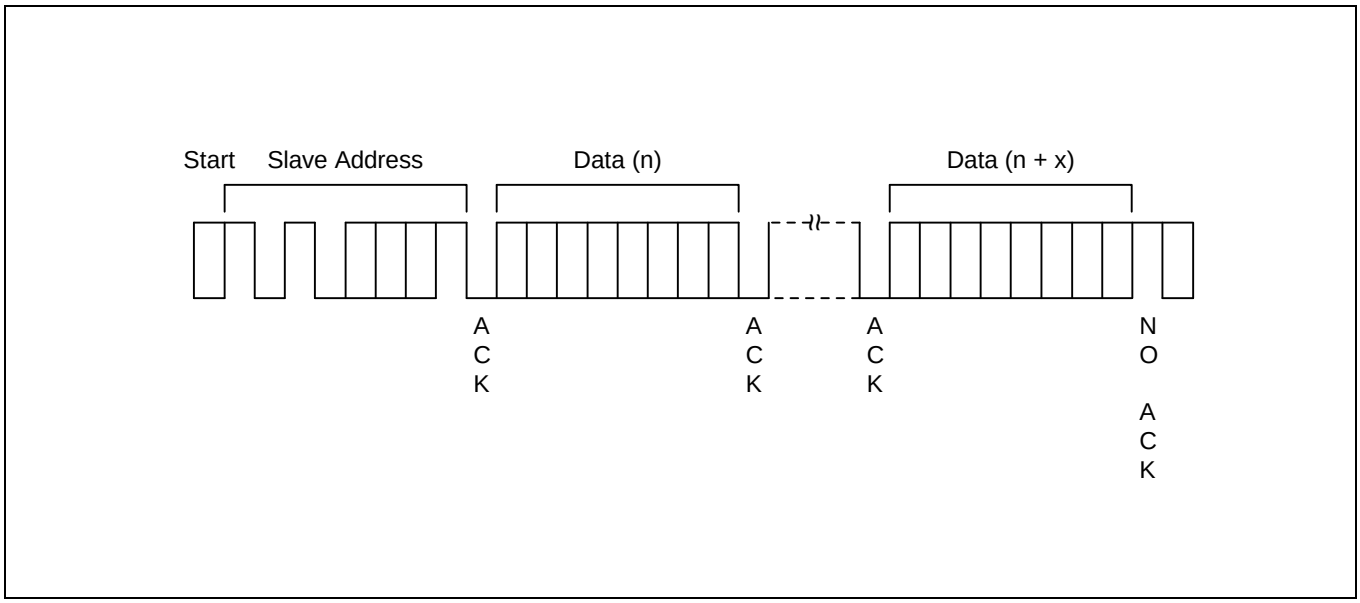


Figure 3-14. Sequential Read Operation

ELECTRICAL DATA

Table 3-3. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{CC}	–	– 0.3 to + 7.0	V
Input voltage	V_{IN}	–	– 0.3 to + 7.0	V
Output voltage	V_O	–	– 0.3 to + 7.0	V
Operating temperature	T_A	–	– 40 to + 85	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C
Electrostatic discharge	V_{ESD}	HBM	5000	V
		MM	500	

Table 3-4. D.C. Electrical Characteristics

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 1.8 V to 5.5 V)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Input low voltage		V_{IL}	SCL, SDA, A0, A1, A2	–	–	0.3 V_{CC}	V
Input high voltage		V_{IH}		0.7 V_{CC}	–	–	V
Input leakage current		I_{LI}	V_{IN} = 0 to V_{CC}	–	–	10	µA
Output leakage current		I_{LO}	V_O = 0 to V_{CC}	–	–	10	µA
Output low voltage		V_{OL}	I_{OL} = 0.15 mA, V_{CC} = 1.8 V	–	–	0.2	V
			I_{OL} = 2.1 mA, V_{CC} = 2.5 V	–	–	0.4	
Supply current	Write	I_{CC1}	V_{CC} = 5.5 V, 400 kHz	–	–	3	mA
		I_{CC2}	V_{CC} = 1.8 V, 100 kHz	–	–	1	
	Read	I_{CC3}	V_{CC} = 5.5 V, 400 kHz	–	–	0.2	
		I_{CC4}	V_{CC} = 1.8 V, 100 kHz	–	–	60	µA
Stand-by current		I_{CC5}	V_{CC} = SDA = SCL = 5.5 V, all other inputs = 0 V	–	–	5	µA
		I_{CC6}	V_{CC} = SDA = SCL = 1.8 V, all other inputs = 0 V	–	–	1	

Table 3-4. D.C. Electrical Characteristics (Continued)

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	25 °C, 1MHz, V_{CC} = 5 V, V_{IN} = 0 V, A0, A1, A2, SCL and WP pin	–	–	10	pF
Input/output capacitance	$C_{I/O}$	25 °C, 1MHz, V_{CC} = 5 V, $V_{I/O}$ = 0 V, SDA pin	–	–	10	

Table 3-5. A.C. Electrical Characteristics

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	V_{CC} = 1.8 to 5.5 V (Standard Mode)		V_{CC} = 2.5 to 5.5 V (Fast Mode)		Unit
			Min	Max	Min	Max	
External clock frequency	F_{CLK}	–	0	100	0	400	kHz
Clock high time	t_{HIGH}	–	4	–	0.6	–	µs
Clock low time	t_{LOW}	–	4.7	–	1.3	–	
Rising time	t_R	SDA, SCL	–	1	–	0.3	
Falling time	t_F	SDA, SCL	–	0.3	–	0.3	
Start condition hold time	$t_{HD:STA}$	–	4	–	0.6	–	
Start condition setup time	$t_{SU:STA}$	–	4.7	–	0.6	–	
Data input hold time	$t_{HD:DAT}$	–	0	–	0	–	
Data input setup time	$t_{SU:DAT}$	–	0.25	–	0.1	–	
Stop condition setup time	$t_{SU:STO}$	–	4	–	0.6	–	
Bus free time	t_{BUF}	Before new transmission	4.7	–	1.3	–	
Data output valid from clock low (note)	t_{AA}	–	0.3	3.5	–	0.9	
Noise spike width	t_{SP}	–	–	100	–	50	ns
Write cycle time	t_{WR}	–	–	5	–	5	ms

NOTES:

1. Upon customers request, up to 400 kHz (Max.) in standard mode and 1 MHz in fast mode are available.
2. When acting as a transmitter, the TMC 24A01/24A02/24A04/24A08/24A16 must provide an internal minimum delay time to bridge the undefined period (minimum 300 ns) of the falling edge of SCL. This is required to avoid unintended generation of a start or stop condition.

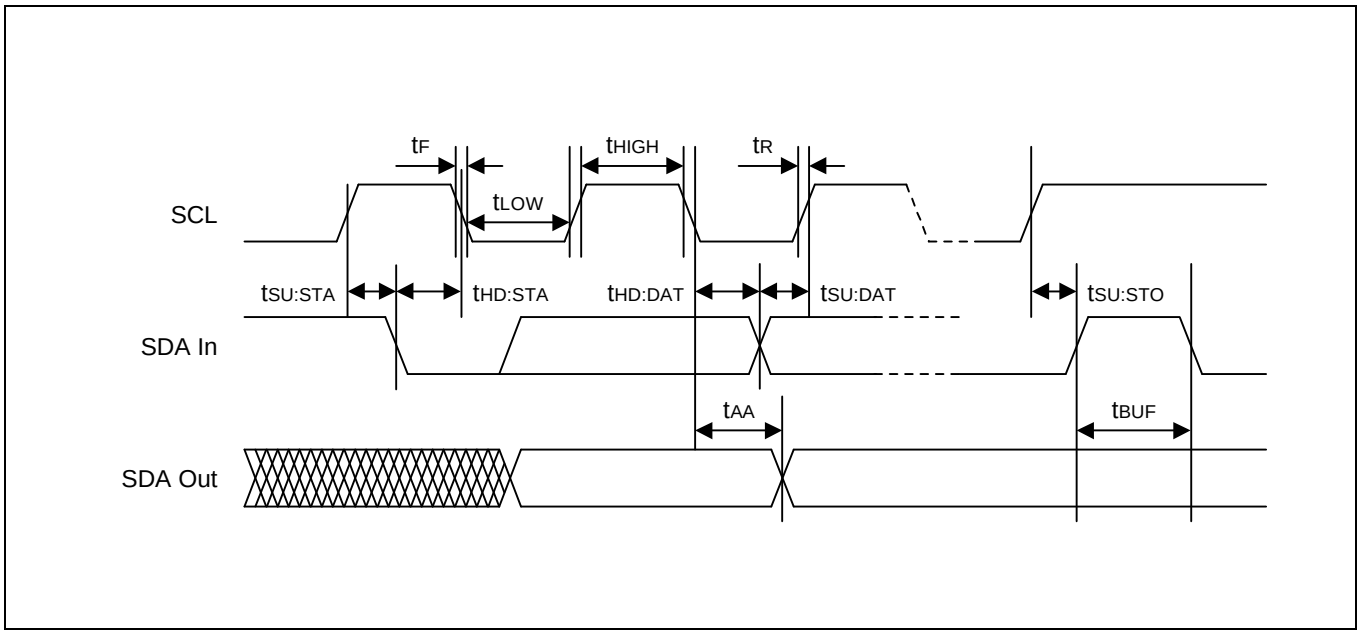


Figure 3-15. Timing Diagram for Bus Operations

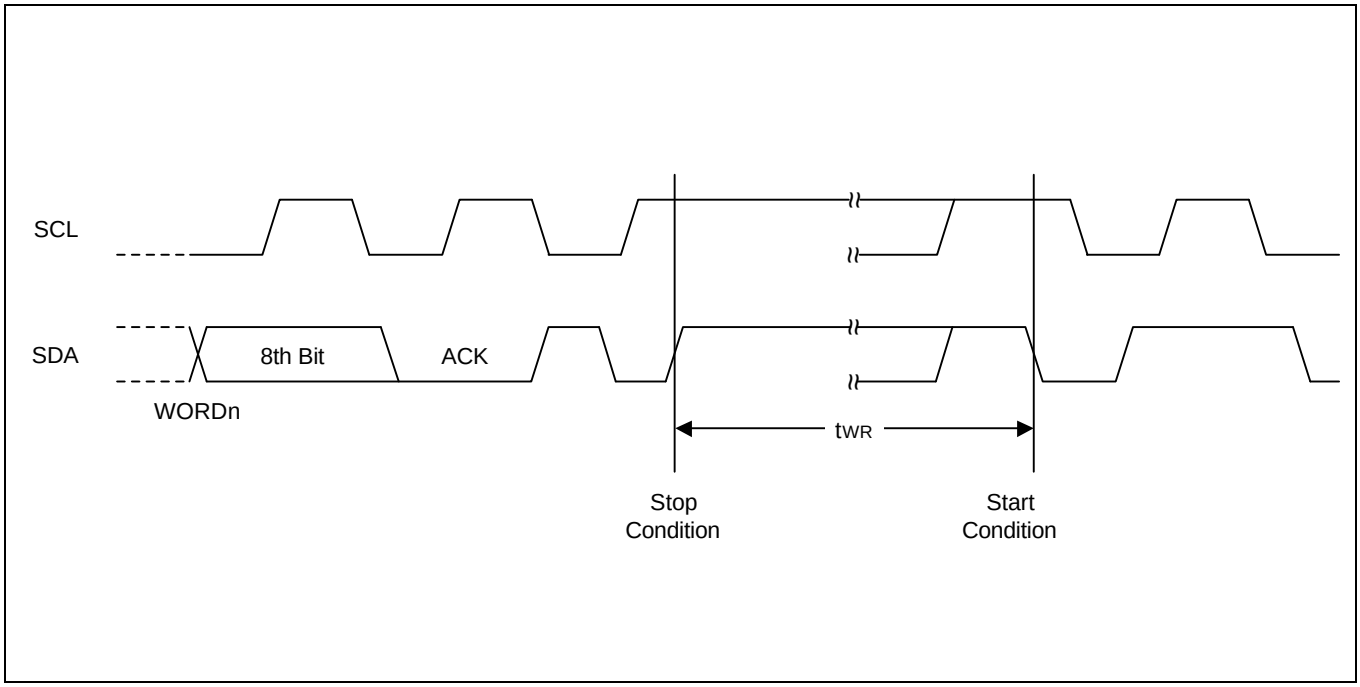
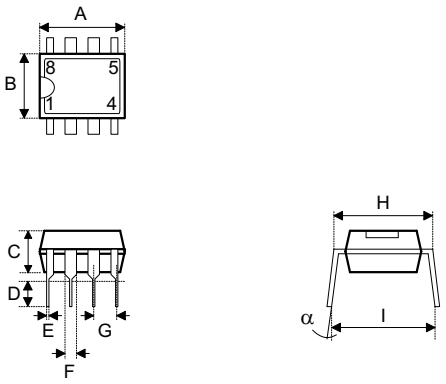


Figure 3-16. Write Cycle Timing Diagram

Plastic DIP Outline Dimensions

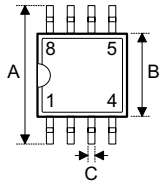
8-pin DIP (300mil) Outline Dimensions

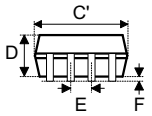


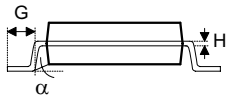
Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	355	—	375
B	240	—	260
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	335	—	375
α	0°	—	15°

SOP Outline Dimensions

8-pin SOP (150mil) Outline Dimensions

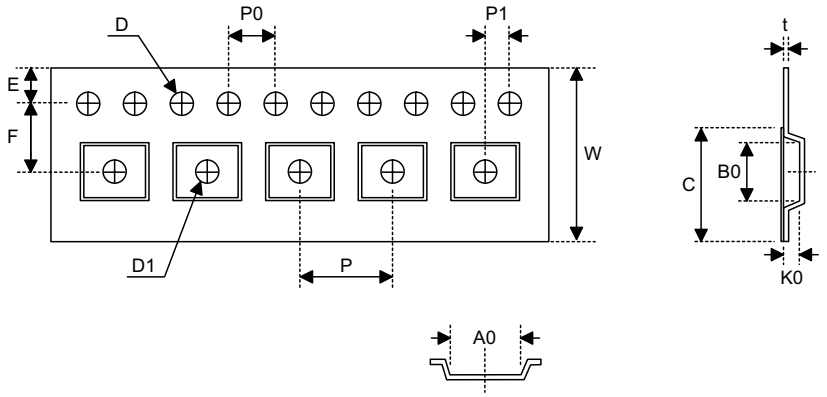






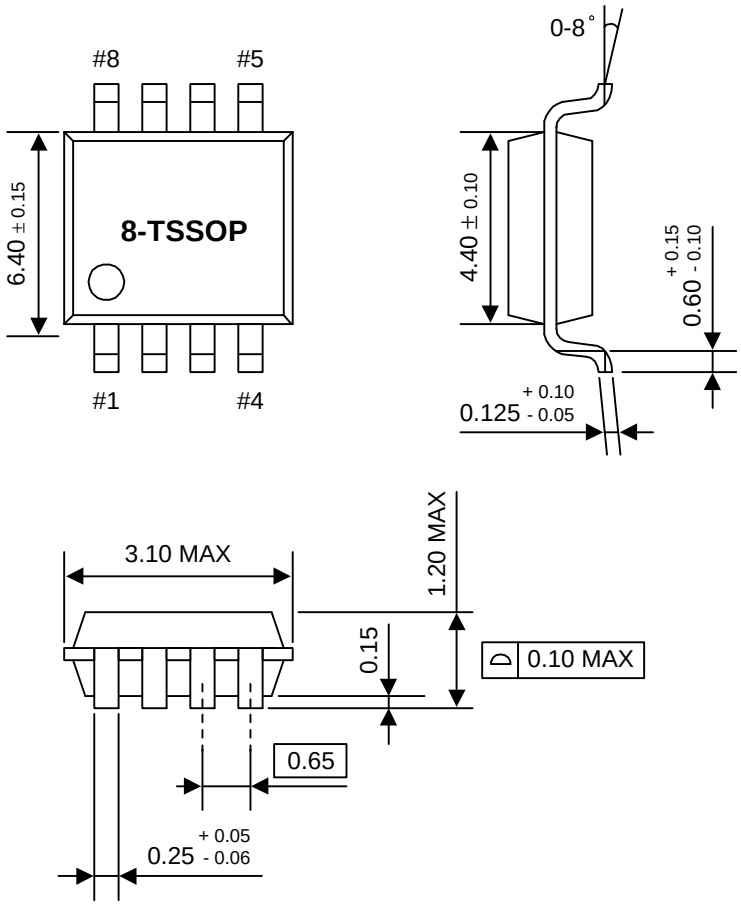
Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	149	—	157
C	14	—	20
C′	189	—	197
D	53	—	69
E	—	50	—
F	4	—	10
G	22	—	28
H	4	—	12
α	0°	—	10°

Carrier Tape Dimensions



SOP 8N

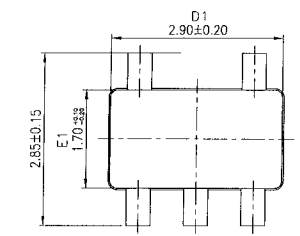
Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0+0.3 −0.1
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.20±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.3±0.05
C	Cover Tape Width	9.3

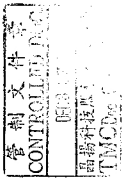


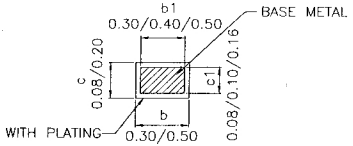
NOTES:

1. Dimensions are in millimeters.

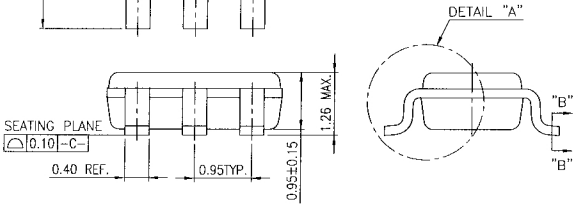
8-TSSOP Package Dimensions

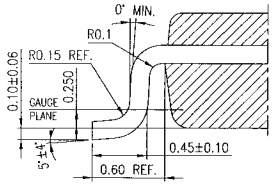






SECTION "B"–"B"





DETAIL "A" (S=32:1)

NOTES:

1. DIMENSION D1 & E1 DOES NOT INCLUDE MOLD PROTRUSION.
2. COPLANARITY OF ALL LEADS SHALL BE (BEFORE TEST) 0.1 MAX. FROM THE SEATING PLANE. UNLESS OTHERWISE SPECIFIED.
3. GENERAL PHYSICAL OUTLINE SPEC IS REFER TO TMC'S FINAL VISUAL INSPECTION SPEC UNLESS OTHERWISE SPECIFIED.

REV.	DESCRIPTION OF REVISION	SIGNATURE/ DATE
3		
2	MODIFY DIM	JANE UOU 99/12/24
1	MODIFY DIM	JANE UOU 99/09/22

晶揚科技股份有限公司
Taiwan Micropag Corporation

TITLE: SOT 25 PACKAGE OUTLINE DWG.

DWG. NO.: EOL-A0050000-001 R2

FILE: EOLA6-001

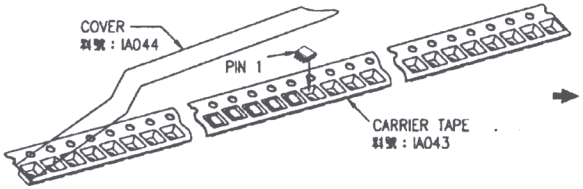
DESIGNER / DATE	MATERIAL	SCALE	
JANE UOU 991224		16 : 1	
CHECKER / DATE	PROCESSES	SHEET NO.	
Robert		1 OF 1	
APPROVED / DATE	UNIT		
	MM		

THIRD ANGLE PROJECTION

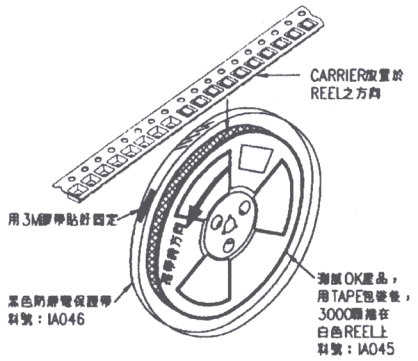
XXXX ±.005
XXX ±.025
XX ±.100
X ±.250
ALL DIMENSIONS IN MILLIMETERS

reel (4992x6996x2 tiff)

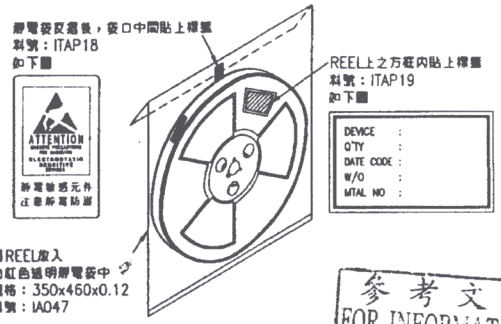
前端空格數	IC產品數	後端空格數
30 格	3000 格	70 格



產品測試完成後與TAPE配置關係

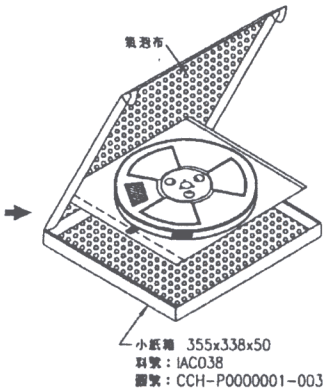


將測試OK產品之TAPE捲到REEL，
外圈再加一黑色防靜電保護帶加以固定

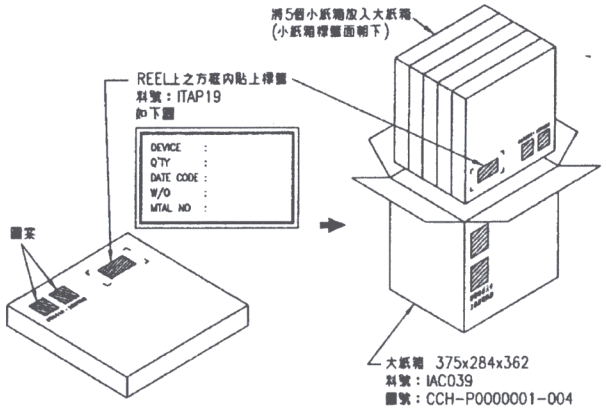


將REEL上方框內貼上標籤，
並放入防靜電袋內

參考文件章
FOR INFORMATION ONLY
JAN 15 2003
晶揚科技股份有限公司
TMC Doc. Control Center

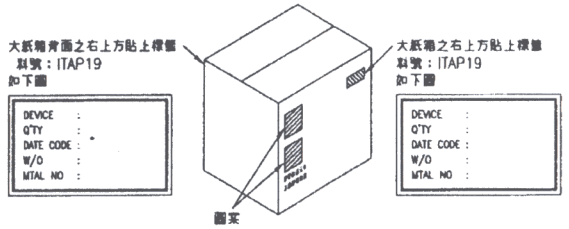


REEL貼標籤面朝上，放入小紙箱內



蓋上小紙箱後，標籤黏貼之位置

5只小紙箱標籤面向下放入大紙箱
不滿5只小紙箱者，仍需以大紙箱包裝
，並以靜電海棉填滿



蓋上大紙箱後以膠帶封合，標籤黏貼之位置

NOTES：1.每一紙箱只能裝同一批產品．
2.同一晶圓批，須同時出貨．
3.尾數箱不能與他批產品併批包裝出貨．
4.測試完不滿3000顆之產品，不以REEL包裝仍以TUBE裝管入庫．

REV.	DESCRIPTION OF REVISION	SIGNATUBE/ DATE
3		
2		
1	增加標示和修改前後空格數．	JANE LIOU. 91/11/06

晶揚科技股份有限公司
Taiwan Micropaq Corporation

TITLE: 晶揚科技SOP 8L TAPE REEL標準包裝規範

DWG. NO. FPK-TMCOP150-004 R1

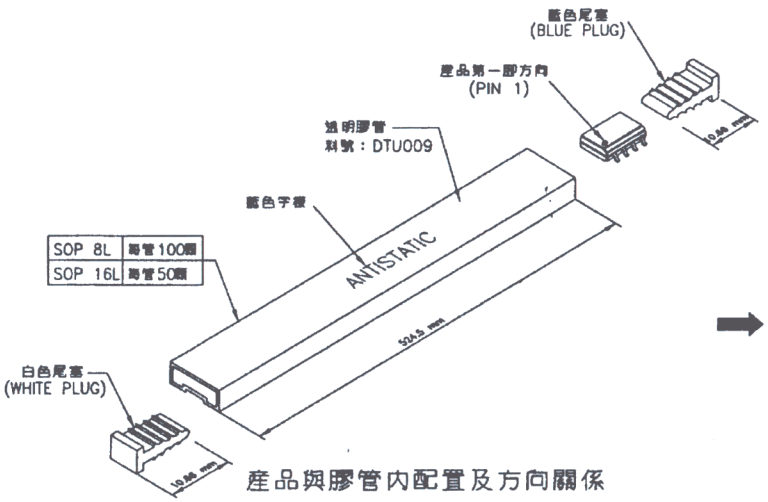
FILE: E:\I晶圓設計圖\包裝規範\FPK-SOP TAPE.DWG

DESIGNER / DATE	MATERIAL	SCALE
JANE LIOU. 91/11/06	~	~
CHECKER / DATE 11/6'02	PROCESSES ~	SHEET NO. 1 OF 1
APPROVED / DATE Harrison 11/6'02	UNIT mm	Q'TY 1

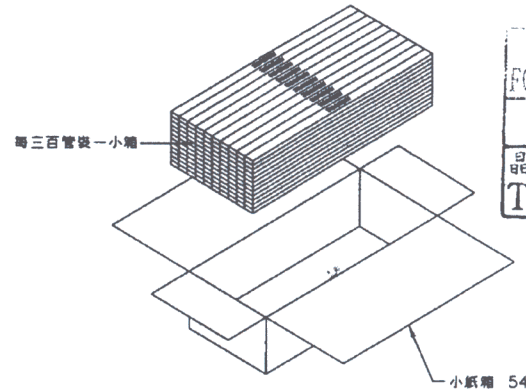
THIRD ANGLE PROJECTION

XXXX ± .005
XXX ± .025
XX ± .100
X ± .250
ALL DIMENSIONS IN MILLIMETERS

sop (4992x6996x2 tiff)

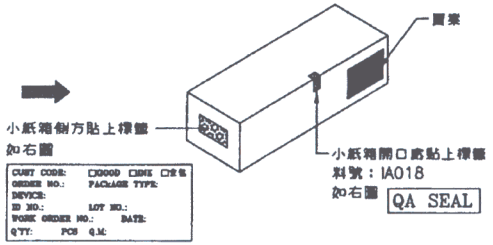


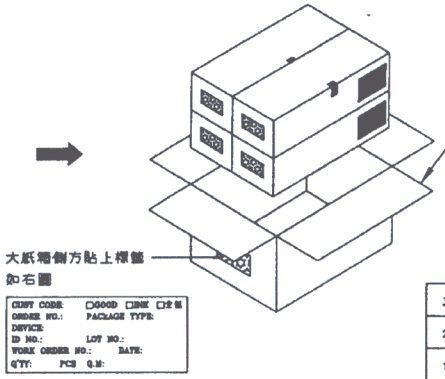
產品與膠管內配置及方向關係



小紙箱 540x162x100
料號：IAC10
圖號：CCH-P0000001-001

將管子放入小紙箱內
藍塞朝內箱標籤面
不需整齊排放





小紙箱標籤黏貼之位置
蓋上小紙箱盒蓋後，以透明膠帶封合

將四只小紙箱放入一只大紙箱內

註：(1) 每一小箱只能裝同一批產品．
(2) 不滿管時須反向放置於包裝箱內．
(3) 同一晶圓批，須同時出貨．
(4) 尾數箱同其包裝方式，小紙箱內之間隙部份亦以防靜電泡綿填充至飽和為止．
(5) 小箱之尾數箱均需以大箱包裝出貨。

FORM:EG00005.C

參考文件章
FOR INFORMATION ONLY
JAN 15 2003
晶揚科技股份有限公司
TMC Doc. Control Center

REV.	DESCRIPTION OF REVISION	SIGNATUBE/ DATE
3	ADD NOTE.	劉昭真 89/06/01
2	MODIFY紙箱	劉昭真 89/04/15
1	ADD NOTE.	劉昭真 11/30/99

晶揚科技股份有限公司
Taiwan Micropaq Corporation

TITLE: 晶揚科技標準包裝規範 FOR SOP 150 MILS.

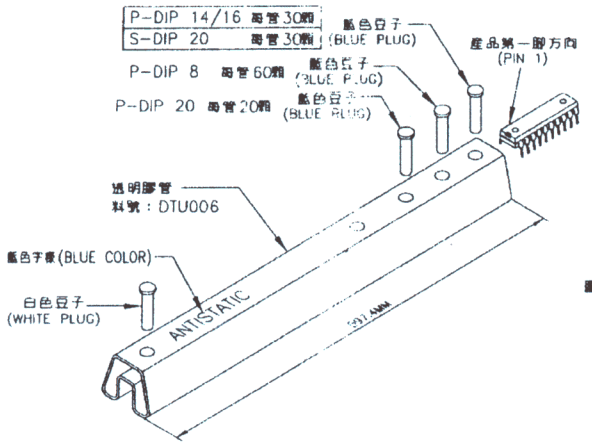
DWG. NO. FPK-TMC0P150-002 R3

FILE FPK-P1503

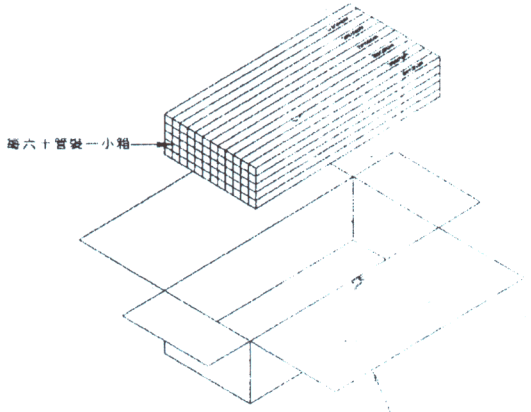
DESIGNER DATE	MATERIAL	SCALE
劉昭真 89/06/01		
CHECKER DATE	PROCESSES	SHEET NO.
C.M.Chang 89/06/01		1 OF 1
APPROVED DATE	UNIT	
Andy 89/6/2		

THIRD ANGLE PROJECTION
.XXXX ±.005
.XXX ±.025
.XX ±.100
.X ±.250
ALL DIMENSIONS IN MILLIMETERS.

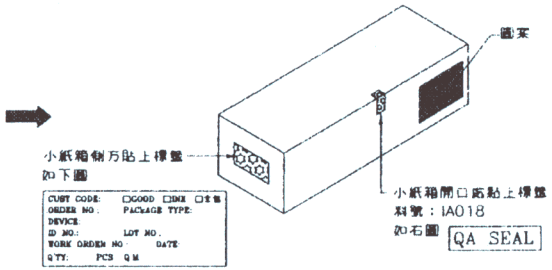
dip (4992x6996x2 tiff)



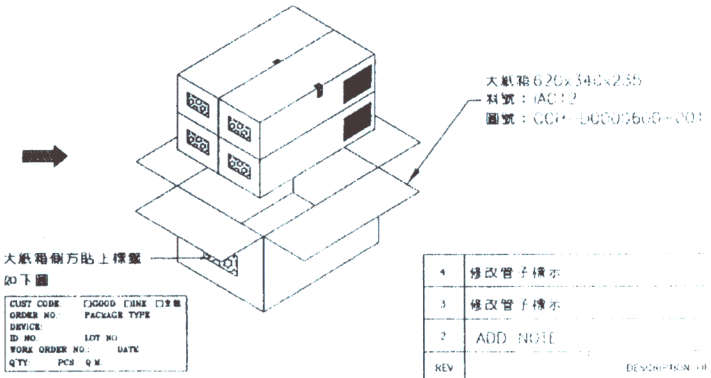
產品與膠管內配置及方向關係



將管子放入小紙箱內
塞塞朝內箱標籤面 不需整齊排放



小紙箱標籤黏貼之位置
蓋上小紙箱盒蓋後，以透明膠帶封合



將四只小紙箱放入一只大紙箱內

考文件
INFORMATION ONLY
JUN 07 2002
晶技股份有限公司
Doc. Control Center

REV	DESCRIPTION OF REVISION	製圖日期
4	修改管子標示	90/11/20
3	修改管子標示	90/11/05
2	ADD NOTE	90/10/01
REV		SIGNATURE / DATE

晶揚科技股份有限公司
Taiwan Micropaq Corporation

DWG NO FPK-TMC02300-002 R4
DESIGNER DATE 製圖員 90/11/05
CHECKED 陳力輝
APPROVED DATE Robert 11/6
MATERIAL
PROCESS
UNIT
SCALE
WT. NO

TITLE 晶揚科技標準包裝規範 FOR P-DIP 300MILS
FILE FPK-TMC-02
THIRD ANGLE PROJECTION
ALL DIMENSIONS IN MILLIMETERS
XXXX ±.025
XXX ±.025
XX ±.100
X ±.250

註：(1) 每一小箱只能裝同一批產品。
(2) 不滿管時須反向放置於包裝箱內。
(3) 同一晶圓批，須同時出貨。
(4) 尾數箱同其包裝方式，箱內之間隙部份亦以防靜電泡綿填充至飽和為止。
(5) 小箱之尾數箱均需以大箱包裝出貨。

FORM:EG00005.C