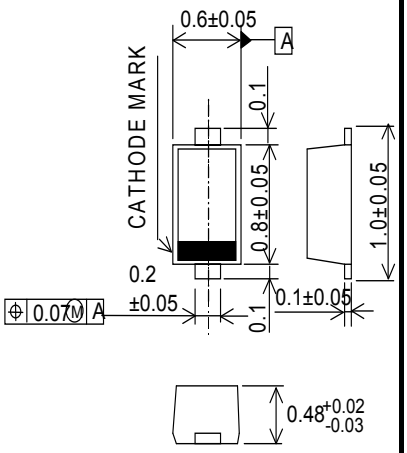
TOSHIBA Diode Silicon Epitaxial Planar Type

1SS427

Ultra-High Speed Switching Applications

- 2-pin compact package: Ideal for high-density mounting
- Low forward voltage: $V_{F\ (3)}$ = 0.98 V (typ.)
- Fast reverse recovery time: t_{rr} = 1.6 ns (typ.)
- Small total capacitance: C_T = 0.5 pF (typ.)

Unit: mm



fSC

JEDEC	—
JEITA	—
TOSHIBA	1-1L1A

Weight: 0.6 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Maximum (peak) reverse voltage	V_{RM}	85	V
Reverse voltage	V_R	80	V
Maximum (peak) forward current	I_{FM}	200	mA
Average forward current	I_O	100	mA
Surge current (10 ms)	I_{FSM}	1	A
Power dissipation	P	150 *	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	−55 to 150	°C

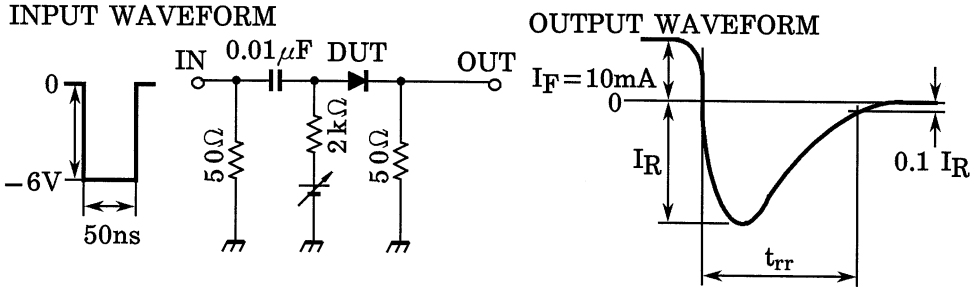
* : Mounted on a glass epoxy circuit board of 20 mm × 20 mm,
Cu pad dimension of 4 mm × 4 mm.

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

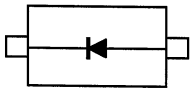
Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_{F\ (1)}$	—	I_F = 1 mA	—	0.62	—	V
	$V_{F\ (2)}$	—	I_F = 10 mA	—	0.75	—	
	$V_{F\ (3)}$	—	I_F = 100 mA	—	0.98	1.20	
Reverse current	$I_{R\ (1)}$	—	V_R = 30 V	—	—	0.1	μA
	$I_{R\ (2)}$	—	V_R = 80 V	—	—	0.5	
Total capacitance	C_T	—	V_R = 0, f = 1 MHz	—	0.5	—	pF
Reverse recovery time	t_{rr}	—	I_F = 10 mA, Fig.1	—	1.6	—	ns

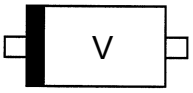
Fig.1 Reverse Recovery Time (t_{rr}) Test Circuit



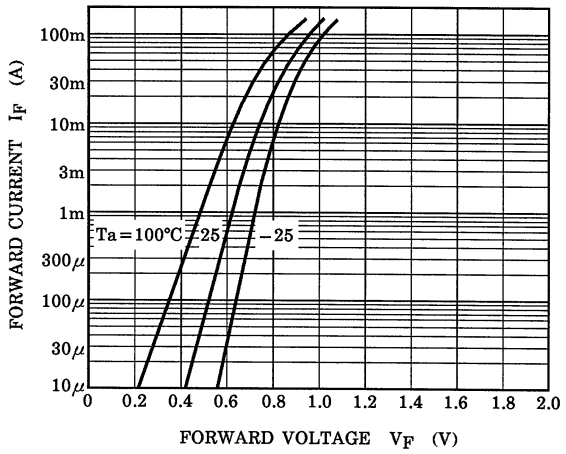
Pin Assignment (top view)



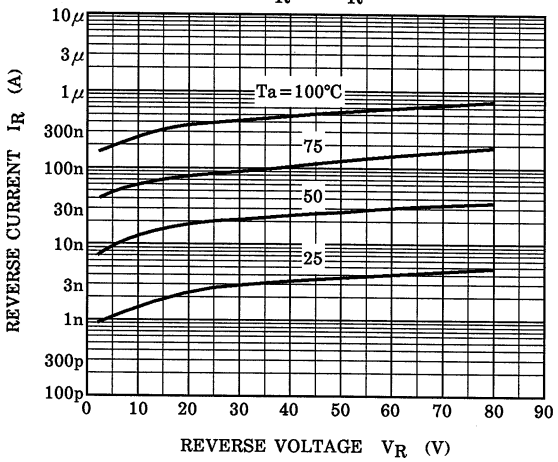
Marking



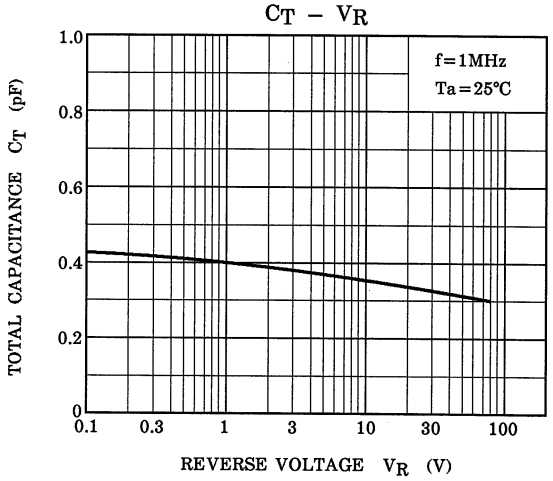
$I_F - V_F$



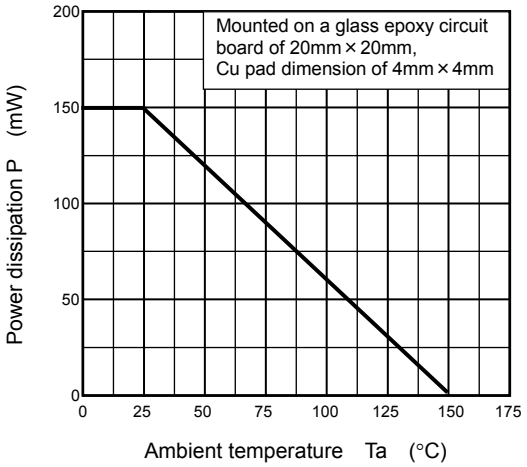
$I_R - V_R$



$C_T - V_R$



P – Ta



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