

5-TAP SMD DELAY LINE

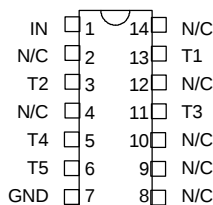
$$T_D/T_R = 3$$

(SERIES 1518)



FEATURES

- 5 taps of equal delay increment
- Delays to 200ns
- Low profile
- Epoxy encapsulated
- Meets or exceeds MIL-D-23859C



PACKAGES

IN Signal Input
T1-T5 Tap Outputs
GND Ground

Note: Standard pinout shown
Alt. pinout available

FUNCTIONAL DESCRIPTION

The 1518-series device is a fixed, single-input, five-output, passive delay line. The signal input (IN) is reproduced at the outputs (T1-T5) in equal increments. The delay from IN to T5 (T_D) and the characteristic impedance of the line (Z) are determined by the dash number. The rise time (T_R) of the line is 30% of T_D , and the 3dB bandwidth is given by $1.05 / T_D$. The device is available in a 14-pin SMD with two pinout options.

Part numbers are constructed according to the scheme shown at right. For example, 1518-101-500A is a 100ns, 50Ω delay line with pinout code A. Similarly, 1518-151-501 a is 150ns, 500Ω delay line with standard pinout.

PART NUMBER CONSTRUCTION

1518 - xxx - zzz p

DELAY TIME

Expressed in nanoseconds (ns)
First two digits are significant figures
Last digit specifies # of zeros to follow

IMPEDANCE

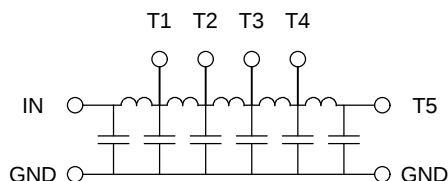
Expressed in nanoseconds (ns)
First two digits are significant figures
Last digit specifies # of zeros to follow

PINOUT CODE

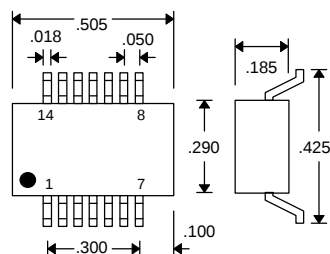
See Table
Omit for STD pinout

SERIES SPECIFICATIONS

- Dielectric breakdown: 50 Vdc
- Distortion @ output: 10% max.
- Operating temperature: -55°C to +125°C
- Storage temperature: -55°C to +125°C
- Temperature coefficient: 100 PPM/°C



Functional Diagram



Package Dimensions

DELAY SPECIFICATIONS

T_D (ns)	T_i (ns)	T_R (ns)	ATTENUATION (%) TYPICAL				
			Z=50Ω	Z=100Ω	Z=200Ω	Z=300Ω	Z=500Ω
5	1.0	3.0	N/A	5	N/A	N/A	N/A
10	2.0	4.0	3	5	5	N/A	N/A
15	3.0	5.0	3	5	5	N/A	N/A
20	4.0	6.0	3	5	5	5	N/A
25	5.0	7.0	3	5	5	5	7
30	6.0	10.0	3	5	5	5	7
40	8.0	13.0	3	5	5	5	7
50	10.0	15.0	3	5	5	7	7
60	12.0	20.0	3	5	6	7	8
75	15.0	25.0	3	5	6	7	8
80	16.0	26.0	4	5	6	7	8
100	20.0	30.0	4	5	6	7	8
110	22.0	32.0	4	5	6	7	8
125	25.0	40.0	4	5	6	7	8
150	30.0	50.0	N/A	5	8	10	10
180	36.0	60.0	N/A	7	8	10	10
200	50.0	70.0	N/A	8	10	12	12

Notes: T_i represents nominal tap-to-tap delay increment
Tolerance on $T_D = \pm 5\%$ or $\pm 2\text{ns}$, whichever is greater
Tolerance on $T_i = \pm 5\%$ or $\pm 1\text{ns}$, whichever is greater
"N/A" indicates that delay is not available at this Z

PINOUT CODES

CODE	IN	T1	T2	T3	T4	T5	GND
STD	1	13	3	11	5	6	7
A	1	12	4	10	6	7	8,14

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PASSIVE DELAY LINE TEST SPECIFICATIONS

TEST CONDITIONS

INPUT:

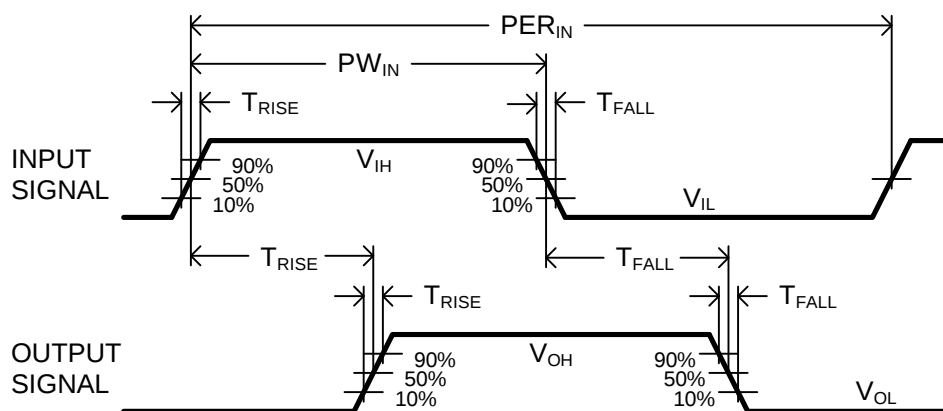
Ambient Temperature: $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$
Input Pulse: High = 3.0V typical
 Low = 0.0V typical
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured at 10% and 90% levels)

OUTPUT:

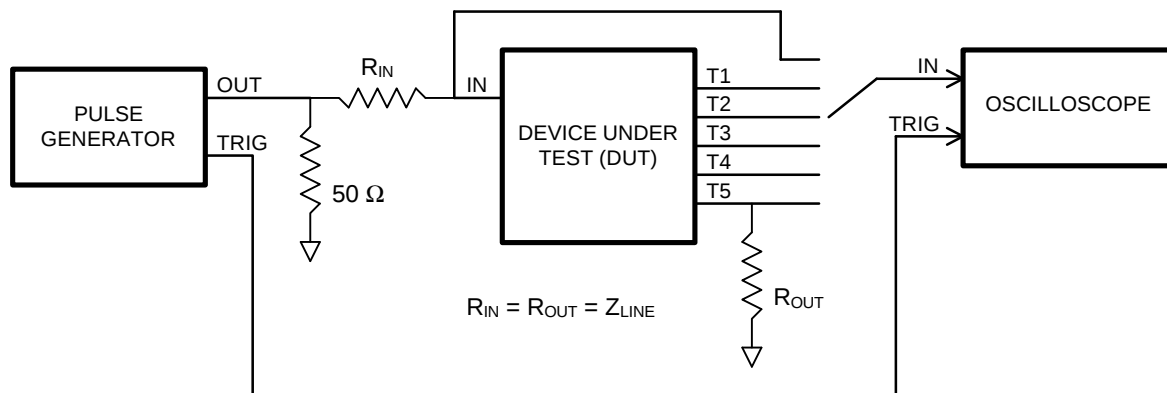
R_{load} : $10\text{M}\Omega$
 C_{load} : 10pf
Threshold: 50% (Rising & Falling)

Pulse Width ($T_D \leq 75\text{ns}$): $PW_{\text{IN}} = 100\text{ns}$
Period ($T_D \leq 75\text{ns}$): $PER_{\text{IN}} = 1000\text{ns}$
Pulse Width ($T_D > 75\text{ns}$): $PW_{\text{IN}} = 2 \times T_D$
Period ($T_D > 75\text{ns}$): $PER_{\text{IN}} = 10 \times T_D$

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Timing Diagram For Testing



Test Setup