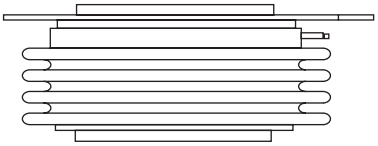
Distributed Gate Thyristors (Hockey PUK Version), 1460A

FEATURES

- Distributed center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AC (K-PUK), Nell's D-type Capsule
- Compliant to RoHS
- Low on-state and switching losses
- Fast turn-on time, $t_{gt} \leq 3\mu s$
- di/dt > 1500 A/μs



TO-200AC(K-PUK)
(Nell's D-type Capsule)

TYPICAL APPLICATIONS

- DC and AC motor controls
- Controlled DC power supplies
- AC controllers
- Ideal for Impulse Magnetizer

PRODUCT SUMMARY	
$I_{T(AV)}$	1460A

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNIT
$I_{T(AV)}$	Double side cooled, single phase, 50Hz, 180° half-sine wave	1460	A
	T_{hs}	55	°C
$I_{T(RMS)}$		2900	A
	T_{hs}	25	°C
I_{TSM}	50 HZ	20	kA
	60 HZ	21	
I^2t	50 HZ	2000	kA^2s
	60 HZ	1830	
V_{DRM}/V_{RRM}		1600 to 3200	V
t_{gt}	Typical	2.0	μs
T_q	Maximum	250	
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{DRM}/I_{RRM}, MAXIMUM AT $T_J = T_J$ MAXIMUM mA
1460PTGxxD0	16	1600	1700	100
	18	1800	1900	
	20	2000	2100	
	24	2400	2500	
	26	2600	2700	
	30	3000	3100	
	32	3200	3300	

FORWARD CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNIT
Maximum average current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled			1460(630)	A
					55/(85)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25°C heatsink temperature double side cooled			2900	A
Maximum peak, one cycle non-reptitive surge current	I_{TSM}	t = 10ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	20	A
		t = 8.3ms			21	
		t = 10ms	100%V_{RRM} reapplied		16.8	
		t = 8.3ms			17.6	
Maximum I^2t for fusing	I^2t	t = 10ms	No voltage reapplied		2000	kA^2s
		t = 8.3ms			1830	
		t = 10ms	100%V_{RRM} reapplied		1411	
		t = 8.3ms			1286	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			20000	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			1.25	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			1.50	
Low level value on-state slope resistance	r_{t1}	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.48	mΩ
High level value on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.44	
Maximum on-state voltage	V_{TM}	I_{pk} =3000A, $T_J = T_J$ maximum, t_p = 10 ms sine pulse			2.90	V
Maximum holding current	I_H	T_J = 25°C, anode supply 12V resistive load			1000	mA
Typical latching current	I_L				1500	

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Minimum non-repetitive rate of rise of turned-on current	dI/dt	V_D = 67% V_{DRM}, I_{FG} = 2A, T_{case} =125°C	1500	A/μs
Typical turn-off time	t_q	I_{TM} = 1000A, $T_J = T_J$ maximum, dI/dt = 60A/μs. V_R = 50V, dV/dt = 20 V/μs, V_{DR} = 33% V_{DRM}, t_p = 1000μs	200	μs
Maximum gate controlled turn-on delay time	t_d	V_D = 67%, V_{DRM}, I_{TM} = 1000A, dI/dt = 60A/μs. I_{FG} = 2A, t_r = 0.5μs, T_J = 25°C	1.6	
Maximum turn-on time	t_{gt}		3.0	
Typical reverse recovery time	t_{rr}		9.5	
Typical recovered charge	Q_{rr}	I_{TM} = 1000A, t_p = 1000μs, dI/dt = 60A/μs. V_R = 50V	3500	μC
Typical reverse recovery current	I_{rm}		315	A

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Minimum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80% rated V_{DRM}	200	V/μs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM},	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	100	mA

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES TYP.	VALUES MAX.	UNIT
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		30		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, f = 50 Hz, d% = 50		5		W
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		3		A
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms		20		V
Maximum peak negative gate voltage	$-V_{GM}$			5		V
DC gate current required to trigger	I_{GT}	T_J = -40°C	Maximum required gate current/voltage are the lowest value which will trigger all units 12V anode to cathode applied	100	-	mA
		T_J = 25°C		50	300	mA
		T_J = 125°C		25	-	mA
DC gate voltage required to trigger	V_{GT}	T_J = -40°C		1.3	-	V
		T_J = 25°C		1.0	3.0	V
		T_J = 125°C		0.8	-	V
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	Maximum gate current/ voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V_{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum operating junction temperature range	T_J		-40 to 125	°C
Maximum storage temperature range	T_{stg}		-40 to 150	°C
Maximum thermal resistance, junction to heatsink	$R_{th(J\text{-}hs)}$	DC operation single side cooled	0.040	K/W
		DC operation double side cooled	0.020	K/W
Maximum thermal resistance, case to heatsink	$R_{th(C\text{-}hs)}$	DC operation single side cooled	0.006	K/W
		DC operation double side cooled	0.003	K/W
Mounting force, ±10%			24500 (2500)	N (kg)
Approximate weight			440	g
Case style		TO-200AC (K-PUK), Nell's D-type Capsule)		

△ R_{thJC} CONDUCTION

CONDUCTION ANGEL	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDUCTIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.003	0.003	0.002	0.002	$T_J = T_J$ maximum	K/W
120°	0.004	0.004	0.004	0.004		
90°	0.005	0.005	0.005	0.005		
60°	0.007	0.007	0.007	0.007		
30°	0.012	0.012	0.012	0.012		

Note

• The table above shows the increment of thermal resistance $R_{thJ\text{-}hs}$ when devices operate at different conduction angles than DC

Fig.1 Current ratings characteristics

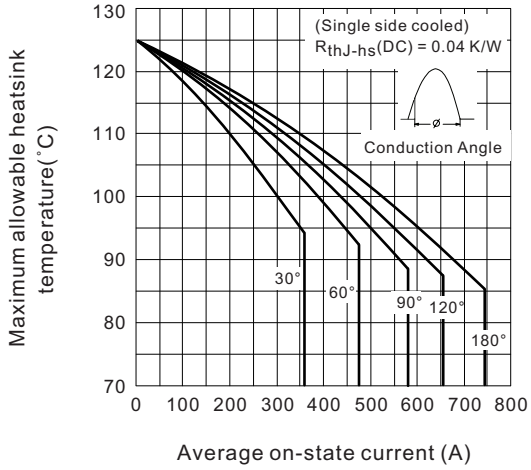


Fig.2 Current ratings characteristics

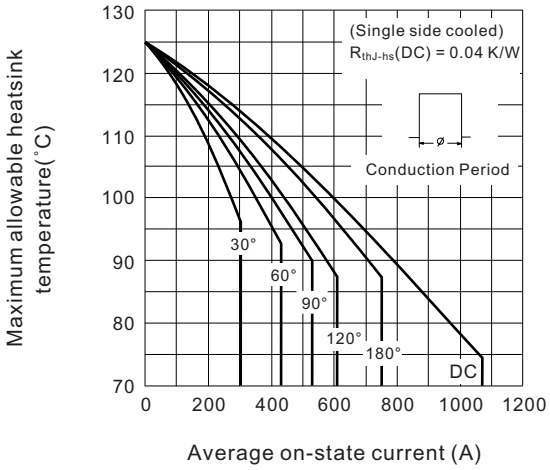


Fig.3 Current ratings characteristics

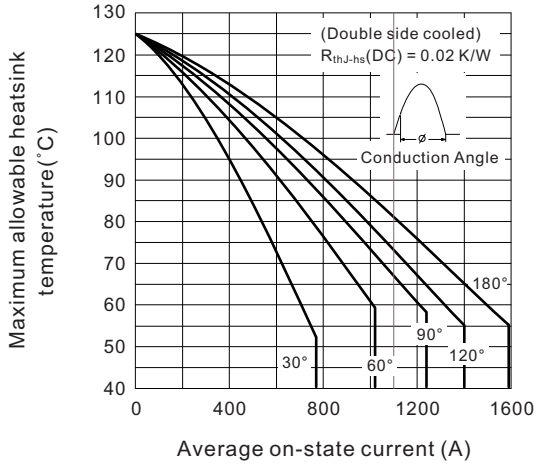


Fig.4 Current ratings characteristics

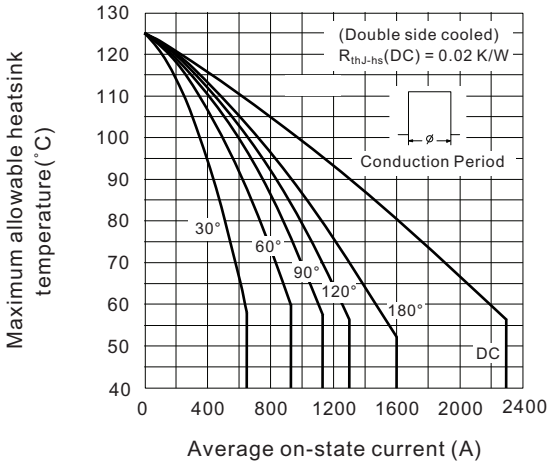


Fig.5 On-state power loss characteristics

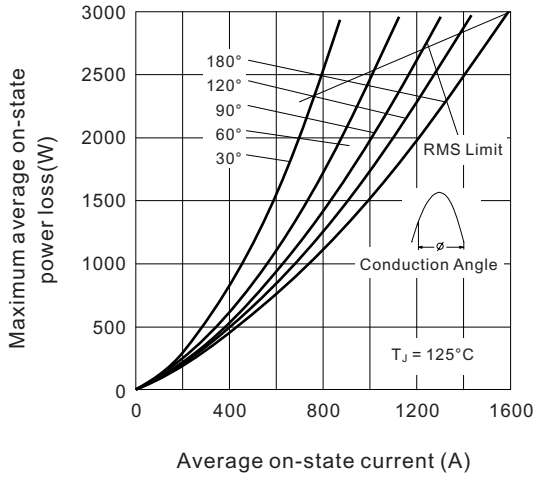


Fig.6 On-state power loss characteristics

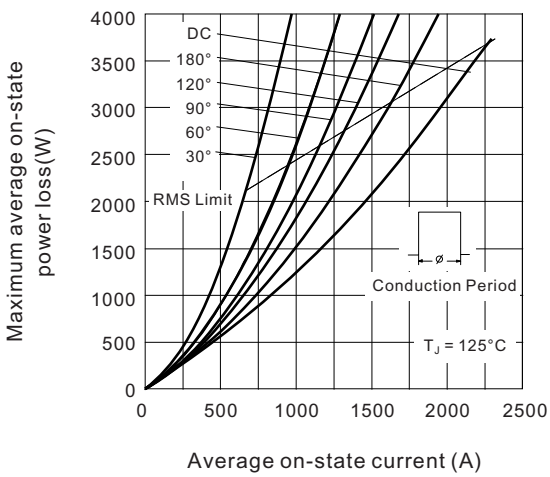


Fig.7 Maximum non-repetitive surge current single and double side cooled

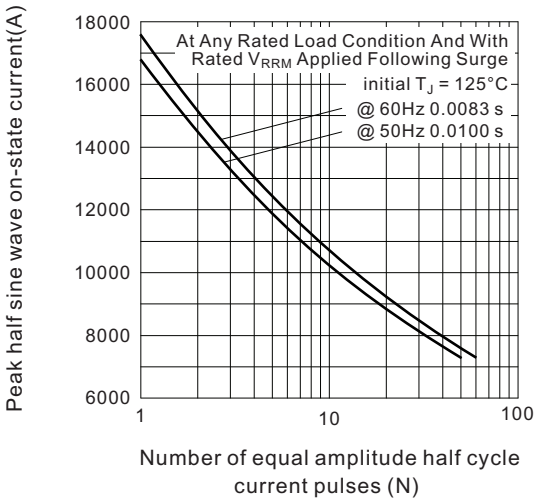


Fig.8 Maximum non-repetitive surge current single and double side cooled

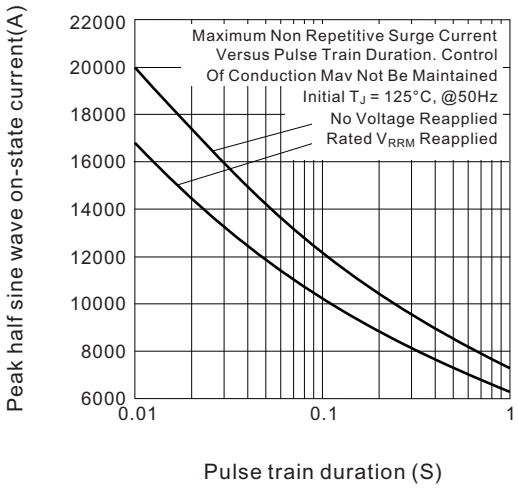


Fig.9 Maximum on-state voltage drop characteristcs

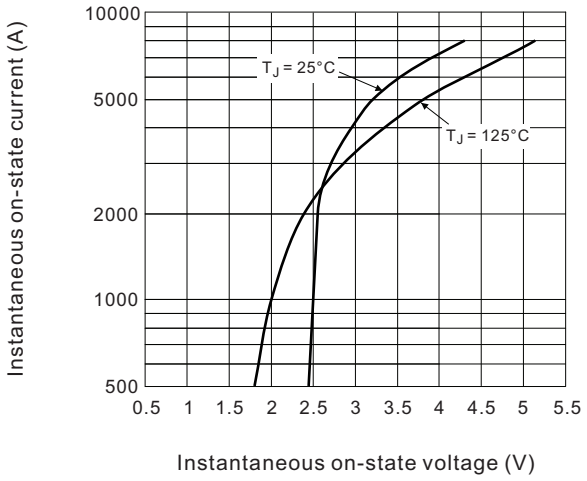


Fig.10 Thermal Impedance $Z_{th(J\text{-}hs)}$ characteristics

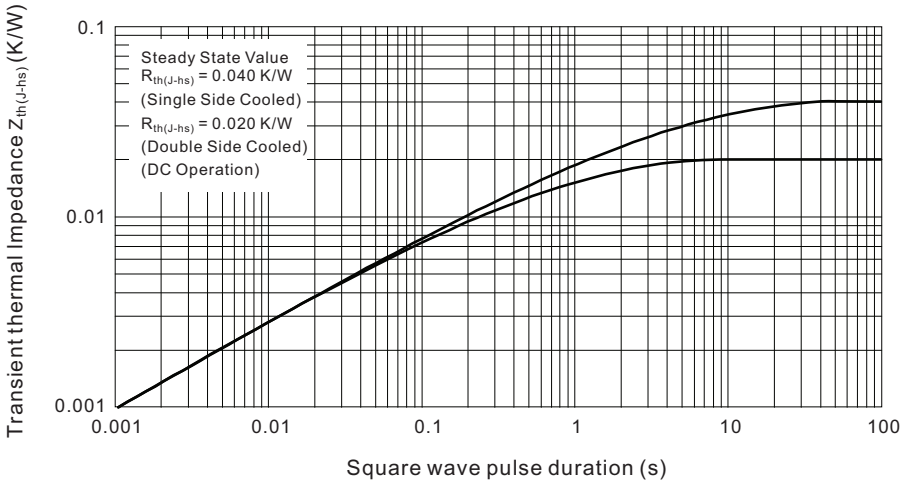


Fig.11 Gate characteristics - Trigger limits

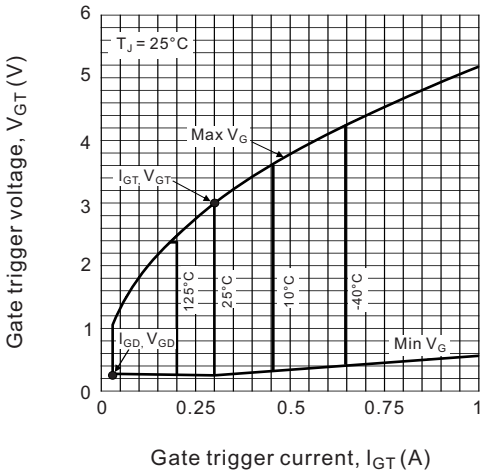


Fig.12 Gate characteristics - Power curves

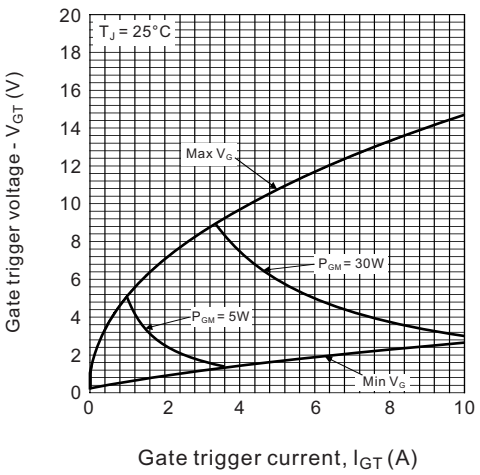


Fig.13 Total recovered charge, Q_{rr}

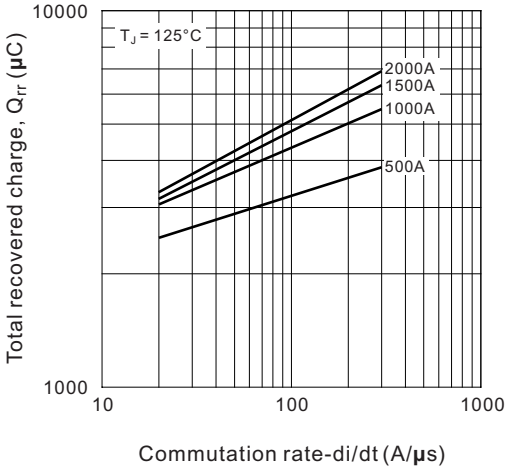


Fig.14 Recovered charge, Q_{ra} (50% chord)

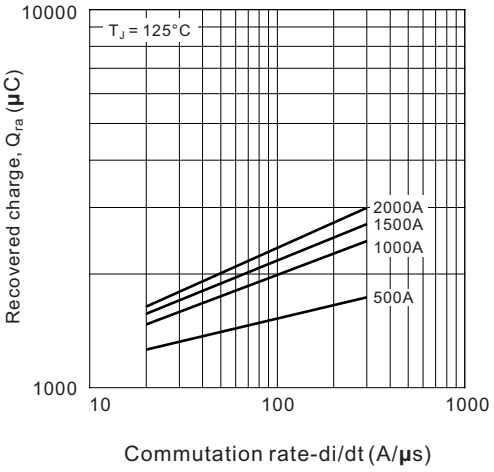


Fig.15 Peak reverse recovery current, I_{rm}

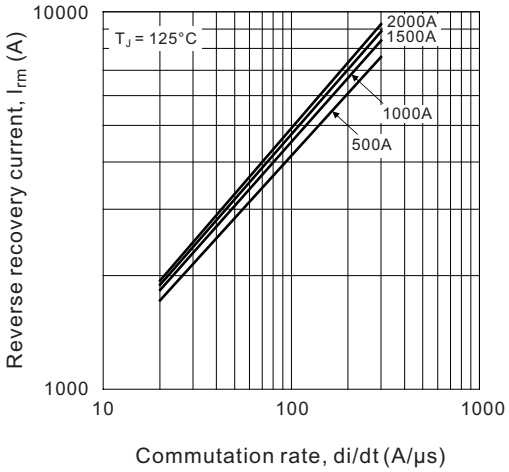


Fig.16 Maximum recovery time, t_{rr} (50% chord)

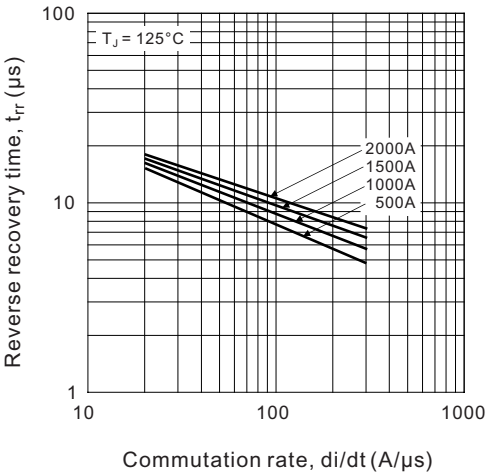


Fig.17 Reverse recovery energy per pulse

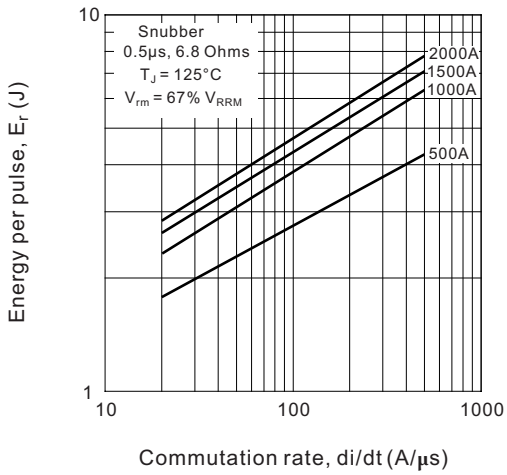
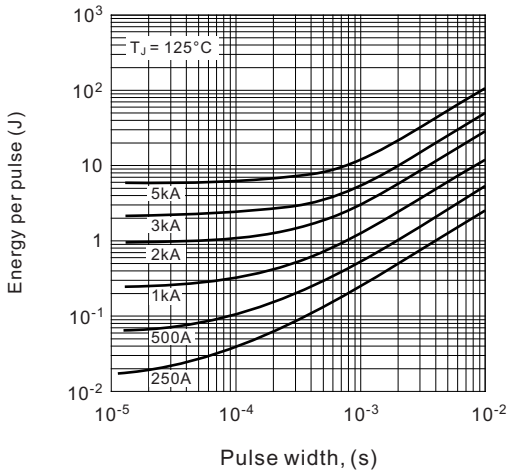


Fig.18 Sine wave energy per pulse



ORDERING INFORMATION TABLE

Device code	1460	PTG	30	D	0
	①	②	③	④	⑤

1 - Maximum average on-state current $I_{T(AV)}$, 1460 for 1460A

2 - PTG = Distribute gate thyristor

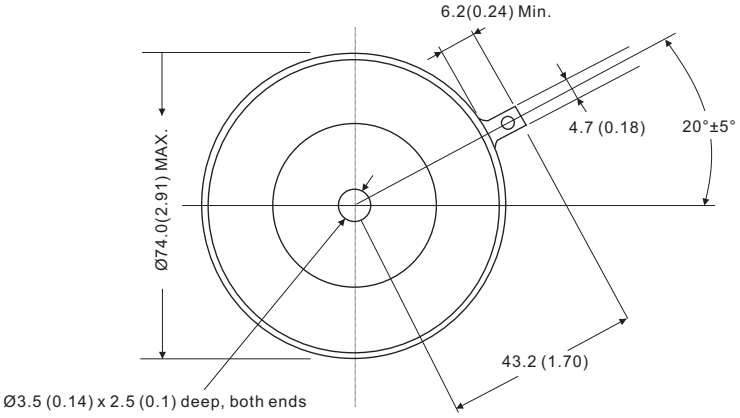
3 - Voltage code, cold × 100 = V_{RRM}/V_{RRM}

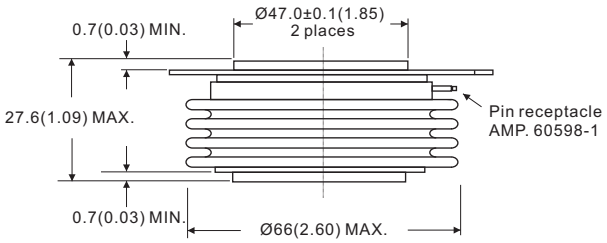
4 - D = PUK case TO-200AC (K-PUK), Nell's D-type Capsule

5 - Terminal type, "0" for eyelet

TO-200AC (K-PUK)

Creepage distance: 28.88(1.137) minimum
Strike distance: 18.0(0.708) minimum







All dimensions in millimeters (inches)