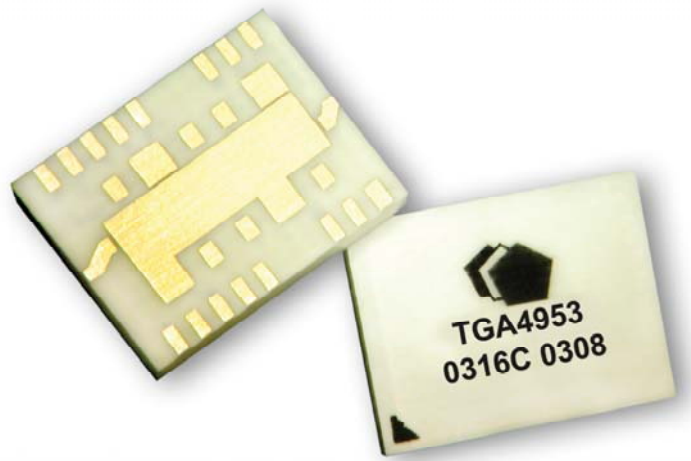


## 9.9-11.2Gb/s Optical Modulator Driver

## TGA4953-EPU

OC-192 Metro and Long Haul Applications

Surface Mount Package



### Description

The TriQuint TGA4953-EPU is part of a series of surface mount modulator drivers suitable for a variety of driver applications and is compatible with Metro MSA standards.

The 4953 consists of two high performance wideband amplifiers combined with off chip circuitry assembled in a surface mount package. A single 4953 placed between the MUX and Optical Modulator provides OEMs with a board level modulator driver surface mount solution.

The 4953 provides Metro and Long Haul designers with system critical features such as: low power dissipation (1.1 W at  $V_o=6$  V), very low rail ripple, high voltage drive capability at 5V bias (6 V amplitude adjustable to 3 V), low output jitter (10 ps typical), and low input drive sensitivity (250 mV at  $V_o=6$  V).

The 4953 requires external DC blocks, a low frequency choke, and control circuitry.

The TGA4953-EPU is available on an evaluation board.

### Key Features and Performance

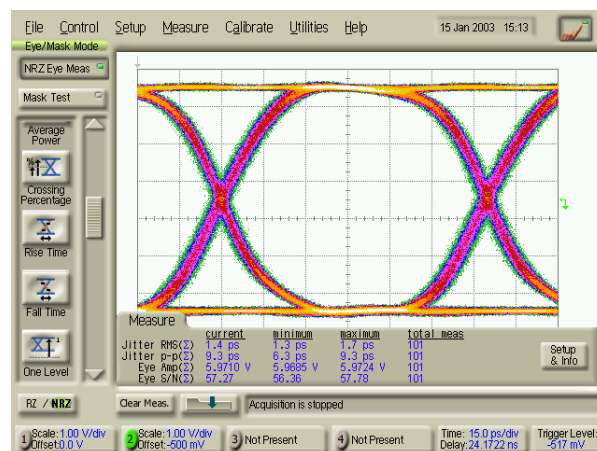
- Metro MSA Compatible
- Wide Drive Range (3V to 10V)
- Single-ended Input / Output
- Low Power Dissipation (1W at  $V_o=6$ V)
- Very Low Rail Ripple
- 25 ps Edge Rates (20/80)
- Small Form Factor
  - 11.4 x 8.9 x 2 mm
  - 0.450 x 0.350 x 0.080 inches
- Evaluation Board Available.

### Primary Applications

- Mach-Zehnder Modulator Driver for Metro and Long Haul.

### Measured Performance

TGA4953 Evaluation Board (Metro MSA Conditions)  
10.7 Gb/s,  $V_{plus}=5$  V,  $I_d=210$  mA, ( $P_{dc}=1.1$  Watt)  
 $V_{out}=6$  Vpp, CPC=50%,  $V_{in} = 500$  mVpp  
Scale: 2 V/div, 15 ps/div



*Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.*

### MAXIMUM RATINGS

| SYMBOL                             | PARAMETER <u>6/</u>                                                                      | VALUE                       | NOTES        |
|------------------------------------|------------------------------------------------------------------------------------------|-----------------------------|--------------|
| Vd1, Vd2T                          | POSITIVE SUPPLY VOLTAGE<br>Drain Voltage                                                 | 8 V                         |              |
| Id1<br>Id2T                        | POSITIVE SUPPLY CURRENT<br>Drain Current<br>Drain Current                                | 100 mA<br>300mA             | <u>1/</u>    |
| P <sub>d</sub>                     | POWER DISSIPATION                                                                        | 4 W                         | <u>2/</u>    |
| Vg1, Vg2<br>Ig1, Ig2               | NEGATIVE GATE<br>Voltage<br>Gate Current                                                 | 0 V to -3 V<br>5 mA         |              |
| Vctrl1, Vctrl2<br>Ictrl1, Ictrl2   | CONTROL GATE<br>Voltage<br>Gate Current                                                  | Vd/2 to -3 V<br>5 mA        | <u>3/</u>    |
| P <sub>IN</sub><br>V <sub>IN</sub> | RF INPUT<br>Sinusoidal Continuous Wave Power<br>10.7Gb/s PRBS Input Voltage Peak to Peak | 23 dBm<br>4 V <sub>pp</sub> |              |
| T <sub>CH</sub>                    | OPERATING CHANNEL TEMPERATURE                                                            | 150 °C                      | <u>4/ 5/</u> |
| T <sub>STG</sub>                   | STORAGE TEMPERATURE                                                                      | -40 to 125 °C               |              |

#### Notes:

- 1/ Assure the combination of Vd and Id does not exceed maximum power dissipation rating.
- 2/ When operated at this bias condition with a base plate temperature of 80°C, the median life is reduced.
- 3/ Assure Vctl1 never exceeds Vd1 and assure Vctrl2 never exceeds Vd2 during bias up and down sequences.
- 4/ These ratings apply to each individual FET.
- 5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 6/ These ratings represent the maximum operable values for the device.

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### THERMAL INFORMATION

| Parameter                                                               | Test Condition                 | P <sub>diss</sub><br>(W) | T <sub>Base</sub><br>(°C) | T <sub>CH</sub><br>(°C) | R <sub>θJC</sub><br>(°C/W) | MTTF<br>(HRS) |
|-------------------------------------------------------------------------|--------------------------------|--------------------------|---------------------------|-------------------------|----------------------------|---------------|
| R <sub>θJC</sub> Thermal Resistance<br>(channel to backside of carrier) | Vd2T=4.7V,<br>Id2T=150mA +/-5% | .71                      | 80                        | 98                      | 26                         | >1E6          |

#### Notes:

1. Based on a detailed thermal model of the output stage where channel temperature is highest. Assumes worst case power dissipation condition (where no RF is applied at the input (no power is dissipated in the load).
2. Thermal transfer is conducted thru the bottom of the TGA4953EPU package into the motherboard. Design the motherboard to assure adequate thermal transfer to the base plate.

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**RF SPECIFICATIONS**

(T<sub>A</sub> = 25°C Nominal)

| NOTE                  | TEST                         | MEASUREMENT CONDITIONS                                        | VALUE                          |     |      | UNITS           |
|-----------------------|------------------------------|---------------------------------------------------------------|--------------------------------|-----|------|-----------------|
|                       |                              |                                                               | MIN                            | TYP | MAX  |                 |
|                       | SMALL SIGNAL BW              |                                                               |                                | 8   |      | GHz             |
|                       | SATURATED POWER BW           |                                                               |                                | 12  |      | GHz             |
| <u>1/</u> , <u>2/</u> | SMALL-SIGNAL GAIN MAGNITUDE  | 2 and 4 GHz<br>6 GHz<br>10 GHz<br>14 GHz<br>18 GHz            | 30<br>28<br>26<br>19<br>12     |     |      | dB              |
|                       | GAIN FLATNESS                | 500KHz thru 5GHz                                              |                                |     | +/-1 | dB              |
|                       | SMALL SIGNAL AGC RANGE       | Midband                                                       |                                | 30  |      | dB              |
|                       | NOISE FIGURE                 | 3 GHz                                                         |                                | 2.5 |      | dB              |
| <u>3/</u> , <u>4/</u> | EYE AMPLITUDE                | VD2T=8.0V<br>VD2T=6.5V<br>VD2T=5.5V<br>VD2T=4.5V<br>VD2T=4.0V | 10<br>8.0<br>7.0<br>6.0<br>5.5 |     |      | V <sub>pp</sub> |
| <u>5/</u>             | ADDITIVE JITTER (rms)        |                                                               |                                | .5  |      | ps              |
| <u>6/</u> , <u>7/</u> | SATURATED OUTPUT POWER       | 2, 4, 6, 8, and 10 GHz                                        | 25                             |     |      | dBm             |
| <u>1/</u> , <u>2/</u> | INPUT RETURN LOSS MAGNITUDE  | 2, 4, 6, 10, 14, and 18GHz                                    | 10                             | 15  |      | dB              |
| <u>1/</u> , <u>2/</u> | OUTPUT RETURN LOSS MAGNITUDE | 2, 4, 6, 10, 14, and 18GHz                                    | 10                             | 15  |      | dB              |
|                       | RISE TIME (20/80)            |                                                               |                                | 25  | 30   | ps              |

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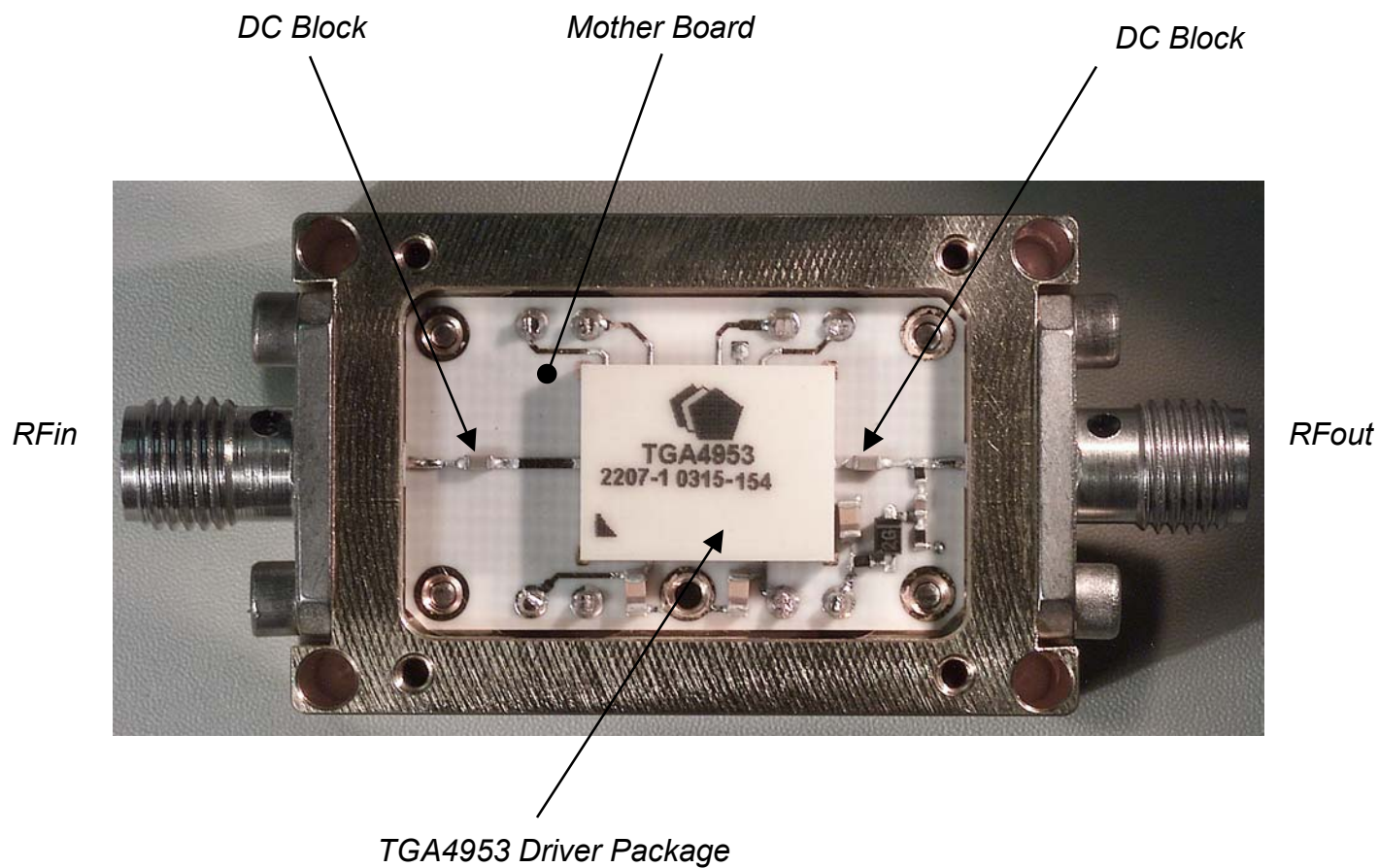
RF SPECIFICATION  
(Continued)

Notes:

- 1/ Verified at package level RF test.
- 2/ Package RF Test Bias:  $V_d=5\text{ V}$ , adjust  $V_{g1}$  to achieve  $I_d=65\text{ mA}$  then adjust  $V_{g2}$  to achieve  $I_d=200\text{ mA}$ ,  $V_{ctrl}=+0.2\text{ V}$
- 3/ Verified by design, SMT assembled onto a demonstration board detailed on sheet 6.
- 4/  $V_{in}=250\text{ mV}$ , Data Rate = 10.7Gb/s,  $VD1=VD2T$  or greater,  $V_{CTRL2}$  and  $V_{G2}$  are adjusted for maximum output.
- 5/ Computed using RSS Method where  $J_{rms\_additive} = \text{SQRT}(J_{rms\_out}^2 - J_{rms\_in}^2)$
- 6/ Verified at die level on-wafer probe.
- 7/ Power Bias Die Probe:  $V_{tee}=8\text{ V}$ , adjust  $V_g$  to achieve  $I_d=175\text{ mA} \pm 5\%$ ,  $V_{ctrl}=1.5\text{ V}$   
Note: At the die level, drain bias is applied thru the RF output port using a bias tee, voltage is at the DC input to the bias tee.

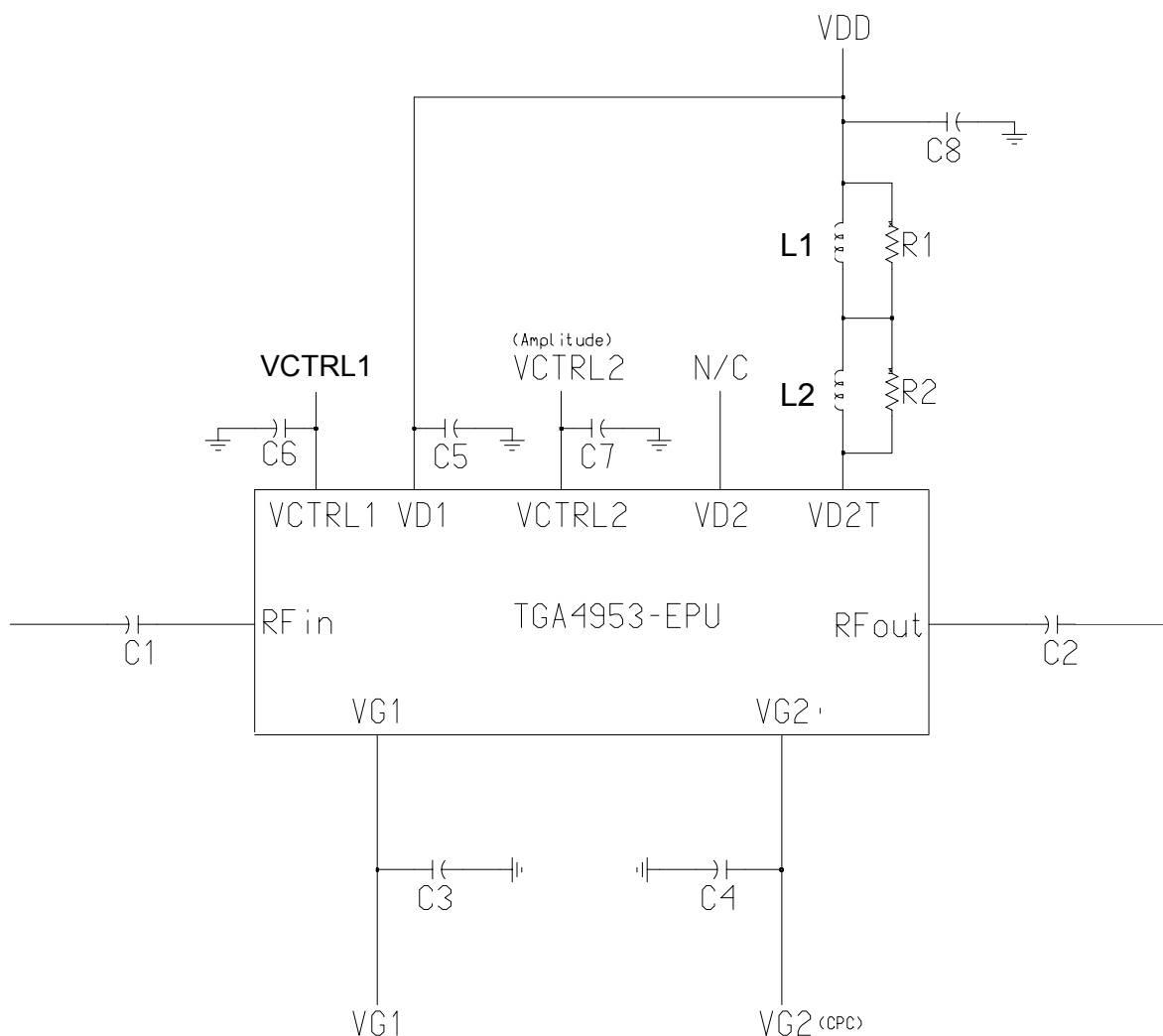
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## Demonstration Board



*Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.*

## Demonstration Board Application Circuit



**Note:**

1. C3 and C4 extend low frequency performance thru 30 KHz. For applications requiring low frequency performance thru 100 KHz, C3 and C4 may be omitted.
2. C5 is a power supply decoupling capacitor and may be omitted.
3. C6 and C7 are power supply decoupling capacitors and may be omitted when driven directly with an op-amp. Impedance looking into VCTRL1 and VCTRL2 is 10Kohms real.

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## Demonstration Board Application Circuit (Continued)

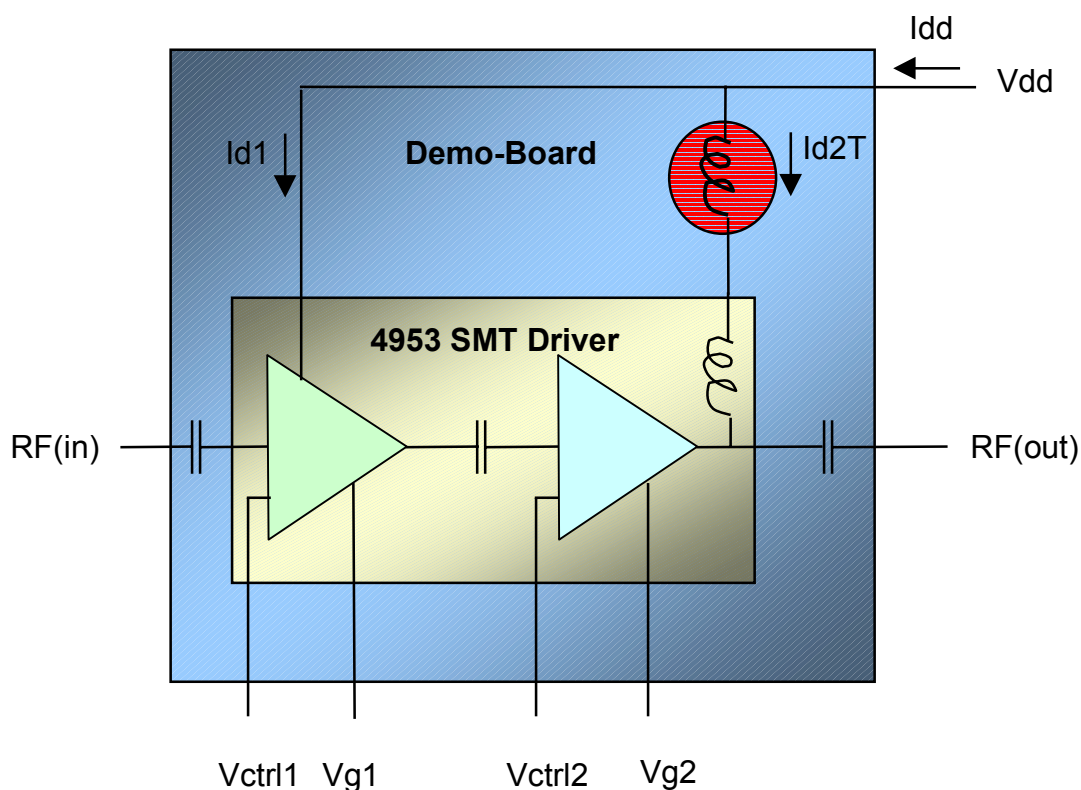
### Recommended Components:

| DESIGNATOR | DESCRIPTION                  | MANUFACTURER | PART NUMBER            |
|------------|------------------------------|--------------|------------------------|
| C1, C2     | DC Block, Broadband          | Presidio     | BB0502X7R104M16VNT9820 |
| C3, C4, C5 | 10uF Capacitor MLC Ceramic   | AVX          | 0802YC106KAT           |
| C6, C7     | 0.01 uFCapacitor MLC Ceramic | AVX          | 0603YC103KAT           |
| C8         | 10 uF Capacitor Tantalum     | AVX          | TAJA106K016R           |
| L1         | 220 uH Inductor              | Belfuse      | S581-4000-14           |
| L2         | 330 nH Inductor              | Panasonic    | ELJ-FAR33MF2           |
| R1, R2     | 274 $\Omega$ Resistor        | Panasonic    | ERJ-2RKF2740X          |

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## TGA4953 Typical Performance Data Measured on a Demonstration Board

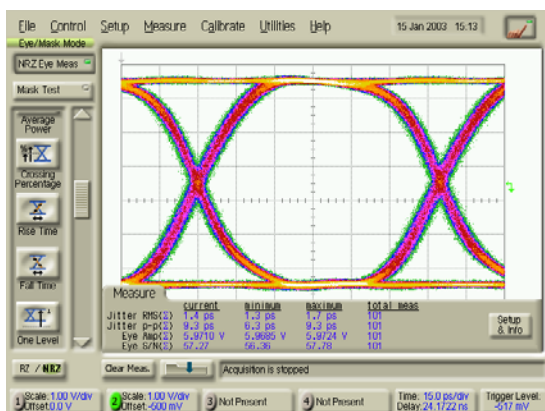


**Demonstration Board Block Diagram**

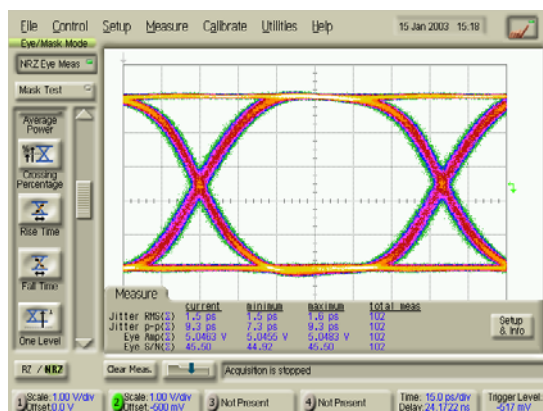
*Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.*

**Typical Measured Performance on Demonstration Board**  
**10.7Gb/s 2<sup>A</sup>31-1, V<sub>dd</sub>=5V**  
**CPC=50%**

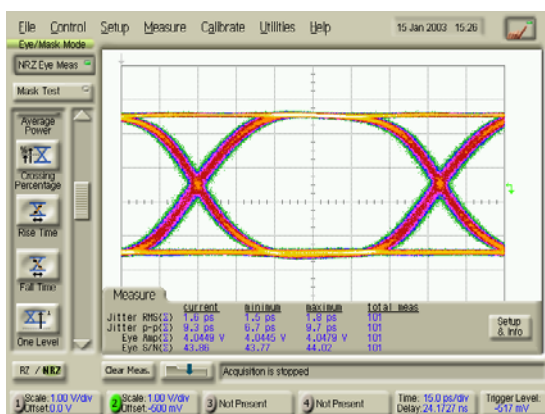
**Vo=6V**



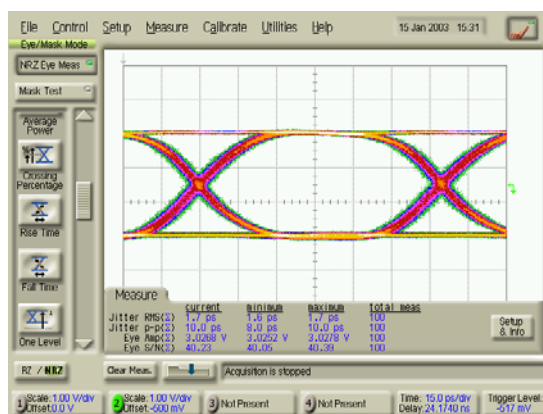
**Vo=5V**



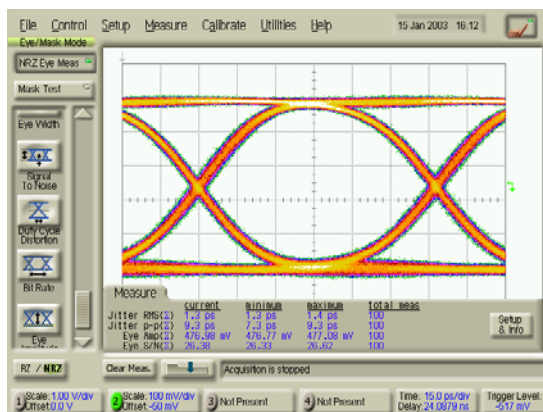
**Vo=4V**



**Vo=3V**



**Input Signal Vin=500mV**



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**Typical Bias Conditions**  
**Vdd=5V**

| Vo(V) | Vg1(V) | Vg2(V) | Id  | Vctrl2 |
|-------|--------|--------|-----|--------|
| 6     | -0.66  | -0.57  | 221 | +0.22  |
| 5     | -0.66  | -0.59  | 198 | +0.04  |
| 4     | -0.66  | -0.67  | 172 | -0.14  |
| 3     | -0.66  | -0.74  | 147 | -0.34  |

**Notes:**

1. Vdd=5V, Id1=65mA, and Vctrl1=-0.2V
2. Vin=500mVpp
3. 50%CPC

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## Bias Procedure

**Vdd=5V, Vo=6Vamp, CPC=50%**

### Bias ON

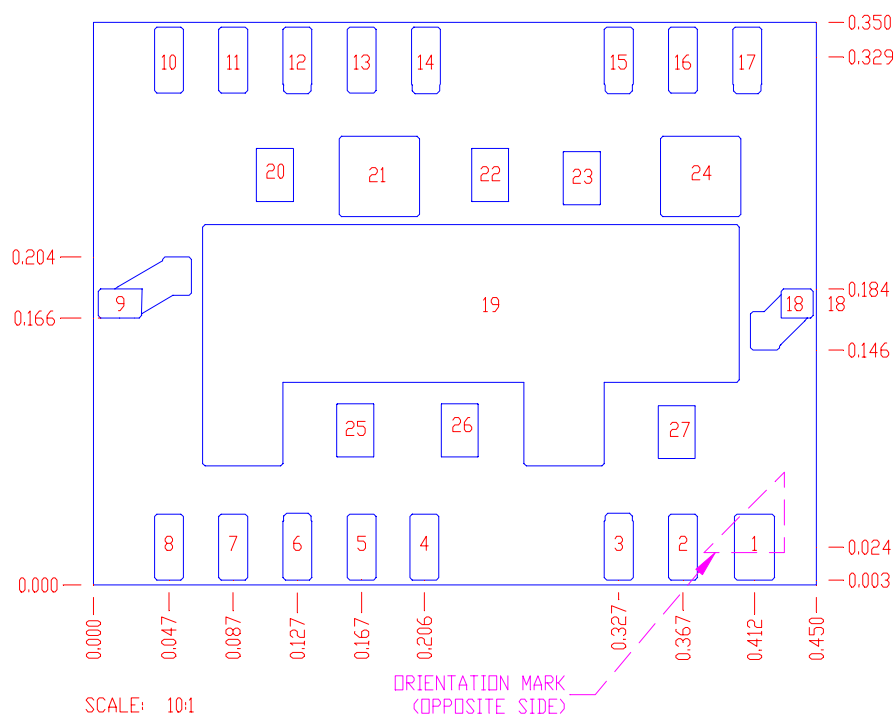
1. Disable the output of the PPG
2. Set Vd=0V Vctrl1=0V Vctrl2=0V Vg1=0V and Vg2=0V
3. Set Vg1=-1.5V Vg2=-1.5V **Vctrl1=-0.2V**
4. Increase Vd to 5V observing Id.
  - Assure Id=0mA
5. Set Vctrl2=+0.2V
  - Id should still be 0mA
6. Make Vg1 more positive until **Id=65mA**.
  - This is Id1 (current into the first stage)
  - Typical value for **Vg1 is -0.65V**
7. Make Vg2 more positive until Id=220mA.
  - This sets Id2T to 155mA.
  - Typical value for Vg2 is -0.55V
8. Enable the output of the PPG.
  - Set Vin=500mV
9. Output Swing Adjust: Adjust Vctrl2 slightly positive to increase output swing or adjust Vctrl slightly negative to decrease the output swing.
  - Typical value for **Vctrl2 is +0.22V** for Vo=6V.
10. Crossover Adjust: Adjust Vg2 slightly positive to push the crossover down or adjust Vg2 slightly negative to push the crossover up.
  - Typical value for **Vg2 is -0.57V** to center crossover with Vo=6V.

### Bias OFF

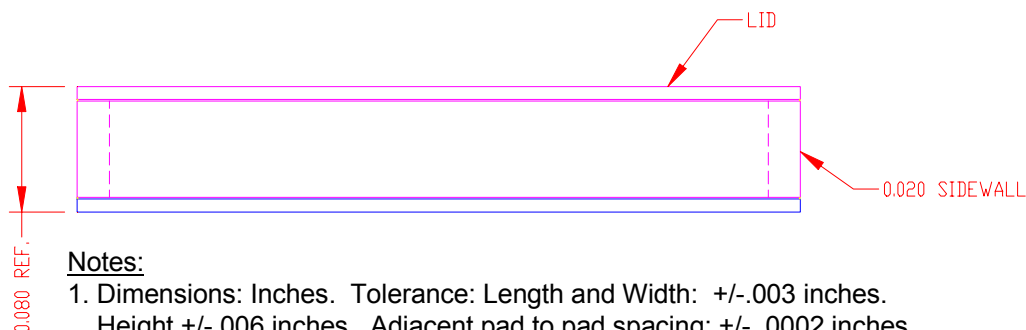
1. Disable the output of the PPG
2. Set Vctrl2=0V
3. Set Vd=0V
4. Set Vctrl1=0V
5. Set Vg2=0V
6. Set Vg1=0V

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## TGA4953 Mechanical Drawing



| PIN | FUNCTION                 | PIN        | FUNCTION                 |
|-----|--------------------------|------------|--------------------------|
| 1   | N/C                      | 10         | N/C                      |
| 2   | N/C                      | 11         | N/C                      |
| 3   | VG1 (0.018" x 0.041")    | 12         | VD2T (0.018" x 0.041")   |
| 4   | N/C                      | 13         | VD2                      |
| 5   | N/C                      | 14         | VCTRL2 (0.018" x 0.041") |
| 6   | VG2 (0.018" x 0.041")    | 15         | VD1 (0.018" x 0.041")    |
| 7   | N/C                      | 16         | N/C                      |
| 8   | N/C                      | 17         | VCTRL1 (0.018" x 0.041") |
| 9   | RF OUT (0.058" x 0.038") | 18         | VF IN (0.039" x 0.038")  |
|     |                          | 19 thru 27 | GND                      |



Notes:

1. Dimensions: Inches. Tolerance: Length and Width: +/- .003 inches.  
Height +/- .006 inches. Adjacent pad to pad spacing: +/- .0002 inches.  
Pad Size: +/- .001 inches.
2. Surface Mount Interface:  
Material: RO4003 (thickness=.008 inches), 1/2oz copper (thickness=.0007 inches)  
Plating Finish: 100-350 microinches nickel underplate, with 5-10 microinches  
flash gold overplate.

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